A 3 V Thermostat Circuit

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Abstract

An Integrated Thermostat Circuit is described in this paper. It contains a bandgap reference, a temperature sensor and two hysteresis comparators. Two temperature trip points are generated by dividing down the bandgap voltage reference using three external resistors or an internal resistive network. The temperature sensor circuit generates a voltage proportional to temperature. Two comparators are designed for a 3 degree C internal hysteresis, and their outputs support CMOS/TTL logic levels. The circuit works with a supply voltage of 2.7V to 10V. It shows a trip point accuracy better than 2 degree C at room temperature and 3 degree C over the temperature ranging from -40 degree C to 125 degree C. The temperature sensor output voltage slope is 6.25mV per degree C. The thermostat is fabricated using a standard bipolar process, and packaged in an 8-pin SOT package.

Introduction

Temperature is a critical parameter that needs to be monitored in many electronic systems. Thermistors have long provided a cost-effective solution to electronic temperature sensing needs. A main drawback of thermistors is their non-linearity over temperature requiring some method of linearization. IC thermometers get around this problem by using on-board circuitry to create a linear output that is proportional to temperature in either degrees C or degrees F. The addition of comparators and an adjustable reference allow for an integrated thermostat to be created on one chip. While this straightforward solution has long been available, this paper describes an analog bipolar thermostat that operates off of 2.7V from -40 to +125 degrees C.

Analysis and Design

The sub-circuits of the proposed thermostat IC are analyzed and design equations are given in the following sections.

Start-up Circuit and Biasing *

A simplified schematic of the new start-up and bias circuit is shown in Figure 1. Its unique feature is that it generates supply dependent current through the main bias string consisting of an epi FET J1, Q1, Q2 and R1 until the bandgap reference is turned on. At that point, the startup circuit senses the bandgap and uses its voltage as its reference point for generating the system bias. The bias current flowing through Q4 is given by

$$I_4 = (V_{bg} - V_{be7}) / (R_2 + R_3) \quad (1)$$

Once the circuit starts, Q2 turns off. The total base current of the current source PNP's flowing through Q7 are compensated by the current sense circuit formed by Q5, Q8, Q9 and Q10. (* *Patent Pending*).

Temperature Sensor and Bandgap Reference

The simplified schematic shown in Figure 2 outlines the low voltage sensor and the bandgap reference. In Figure 2, Q1, Q2 and Q3 form a feedback amplifier. Due to different current densities of the input differential pair Q1 and Q2, a PTAT (Proportional To Absolute Temperature) voltage is created across R1. The matched resistors R2 and R3 are used to multiply the PTAT voltage produced across R1, creating two PTAT voltages; Vp1 across R3, and Vp2 at the emitter of Q3. Voltages Vp1 and Vp2 are expressed in Equations 2 and 3 respectively;

$$V_{p1} = (R_3 / R_1)\, V_t \ln(N) \quad (2)$$

$$V_{p2} = \left[\frac{R_1 + R_2 + R_3}{R_1} \right] V_t \ln(N) \quad (3)$$

where N is the emitter ratio of Q1and Q2. Vt is the thermal voltage.

The bandgap voltage is produced by adding the base-emitter voltage of Q4 to Vp1 as given in Equation 4:

$$V_{bg} = V_{be4} + (R_3 / R_1)\, V_t \ln(N) \quad (4)$$

After producing the initial PTAT voltage, Vp2 is dc level shifted by Q6 and further amplified by R4 and R5. An additional function of Q6 is that it adds approximately 2.2 mV/degree C thermal slope to the Vtmp versus Temperature characteristic. The final expression for Vtmp is given in Equation 5:

$$V_{tmp} = \left(1 + \frac{R_4}{R_5}\right)\left(\left[\frac{R_1 + R_2 + R_3}{R_1} \right] V_t \ln(N) - V_{be6} \right)$$

Eqn. (5)

However a slight nonlinearity is also introduced into the characteristic due to the curvature of the base emitter voltage of Q6 at very high and low values of temperature.
In Figure 2, I3, Q10, Q11, R6 set the collector current for Q4 , and I4, I5, Q8, Q9, R7, R8 set the collector current for Q6.

Hysteresis Comparator

The single-output comparator circuit is shown in Figure 3a. The circuit is formed by joining the outputs of two differential-input folded-cascode comparators in a cross-coupled PNP latch subcircuit. The differential current output of the latch is further converted into a single open collector output through the final stage.

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When the voltage Vtmp<Vhi and also Vtmp<Vlo, the transistors Q3, Q6, Q10 and Q7 are off. The transistors Q4, Q11, Q14 are on and Q12 is saturated. Also Q15, Q16, Q17 are off. As Q14 is on and Q17 is off, the comparator output is high. Now consider the case where Vtmp moved high and is between Vlo and Vhi .Since Vtmp > Vlo, Q9 is off, Q10 and Q7 are on. Therefore, the comparator output is still high. It stays high until Vtmp =Vhi. At that point, current through Q5 and Q6 are equal. Then,

$$I_7 = 2\,I_4 \tag{6}$$

which defines the switching point. As soon as Vtmp crosses Vhi , the comparator output switches to low. The output switches back to high when the Vtmp starts falling and it crosses Vlo. The hysteresis is given by:

$$V_{hys} = V_{hi} - V_{lo} \tag{7}$$

The half circuit of the dual output comparator scheme is shown in Figure 3b.The operation of this circuit is similar to the one in Figure 3a. Initially, let us consider the case where Vtmp < Vtset . At this state, Q5, Q3, Q7, Q9 are on and Q6, Q4, Q10, Q11 are off. The comparator output is high. At the switching point:

$$I_4 = 2\,I_3 \tag{8}$$

$$I_{R1} = I_{R2} = I_{R3} = 2I \tag{9}$$

Let $I_3 = I_x$. Then:

$$I_6 = 2I - I_x \tag{10}$$

$$I_5 = I_x \tag{11}$$

Thus,

$$I_4 = 2I - I_x = I_6 \tag{12}$$

From Equations (8) and (12):

$$I_6 = 2\,I_x \tag{13}$$

We can also write:

$$V_{TMP} - V_{Tset} = V_{BE6} - V_{BE5} = V_T \ln(I_6 / I_5) \tag{14}$$

Therefore, from Equations (11), (13) and (14):

$$V_{HYS} = V_{TMP} - V_{Tset} = V_T \ln(2) \tag{15}$$

Set Point Selection Circuit

The Set Point Selection Circuit is a resistive divider network as shown in Figure 4. Two Voltage levels Vhi and Vlo are generated by dividing down the bandgap voltage Vref .In Figure 4, Ra and Rb are almost binary weighted resistors with metal links L1 to L8 . The resistors Rc1 to Rc12 are equal valued resistors with taps Node 1 through Node 13. The resistor Rp is also an almost binary weighted resistor string with metal links L9 to L14 . Node 1 to 13 are the possible connection nodes for nodes i , j, and k. An optimum short or open circuit combination of links L1 to L14 and Node 1 to 13 connection to i , j, and k nodes is determined for a given Vhi and Vlo using a computer program. The voltages Vhi and Vlo are given as:

$$V_{HI} = \left(\frac{[R_B + (13 - k)R + (j - i)R + (R_P / [k - j]R)]}{R_T} \right) V_{REF} \tag{16}$$

$$V_{LO} = \{ [R_A + (13 - k) R] / R_T \} V_{REF} \tag{17}$$

where

$$R_A = R_O + R_1L_1 + R_2L_2 + R_3L_3 + R_4L_4 \tag{18}$$

$$R_B = R_O + R_5L_5 + R_6L_6 + R_7L_7 + R_8L_8 \tag{19}$$

$$R_P = R_9L_9 + \ldots\ldots + R_{14}\,L_{14} \tag{20}$$

$$R_T = R_A + R_B + (j-1)R + (13-k)R + \left(\frac{R_P}{(k - j)R} \right) \tag{21}$$

Experimental Results

The Thermostat circuit described in this article is fabricated using a standard Bipolar process.

The bandgap characteristic of a typical device is shown in Figure 5. The bandgap circuit is trimmed using Zener Zap Trimming techniques. The temperature coefficient is typically 20ppm/degree C.

The Temperature sensor characteristic of a typical device is shown in Fig. 6. It demonstrates a 6.25mV/degree C thermal slope with very little curvature at the high and low end of the operating temperature range.

The comparators show typically 18mV of hysteresis.

Conclusions

A low-voltage thermostat circuit is designed and fabricated using standard bipolar process. The circuit is packaged in an 8-pin SO package. The circuit works from a single 2.7V to 10V power supply. It has a trip point accuracy of 2 degree C at room and 3 degree C over the temperature range of -40 to 125 degree C. The temperature sense output voltage has a 6.25mV/degree C thermal slope. The temperature coefficient of the bandgap is typically 20ppm/degree C.

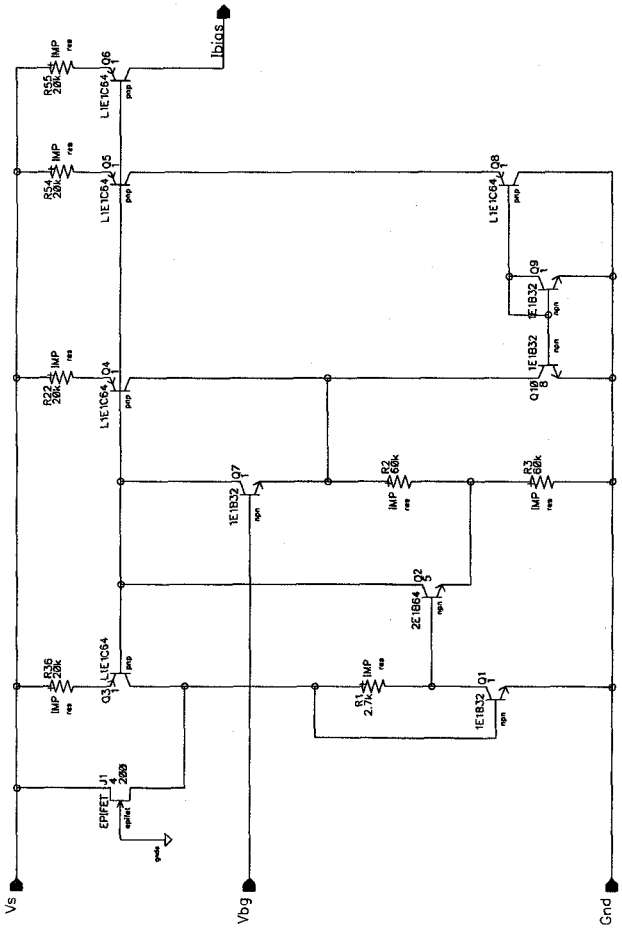

Figure 1

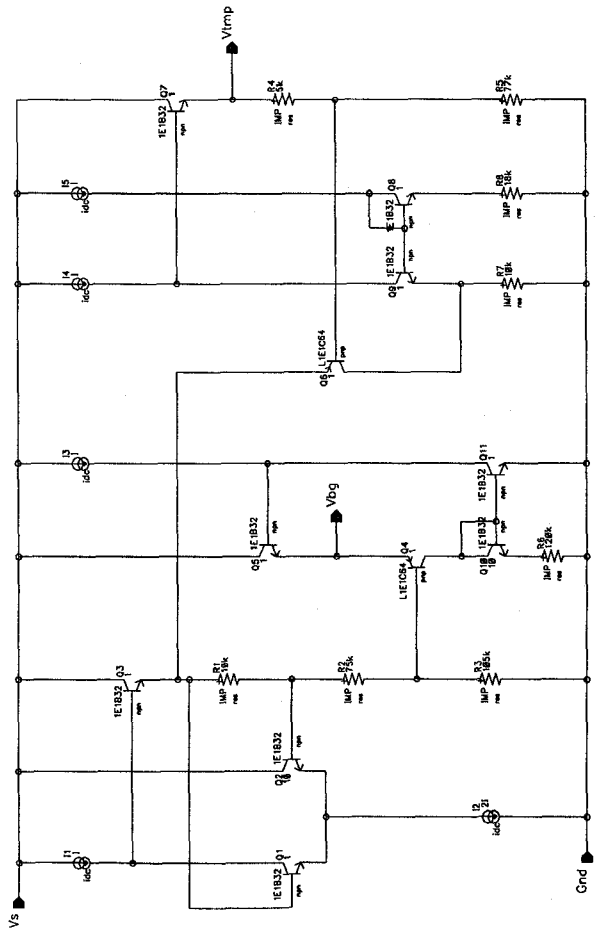

Figure 2

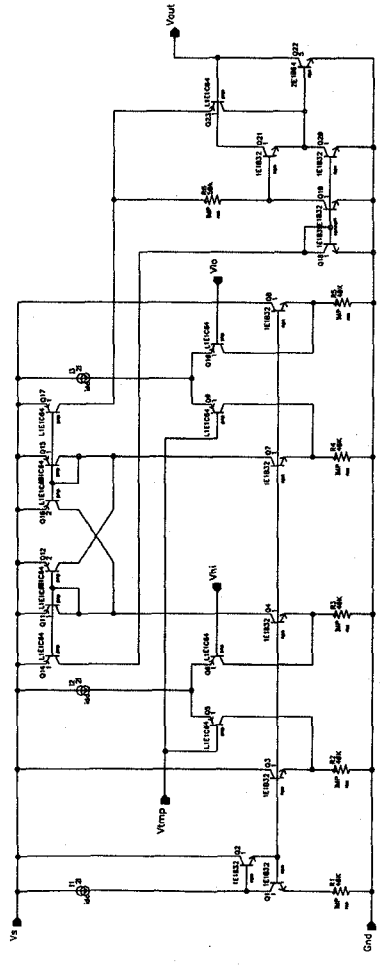

Figure 3b

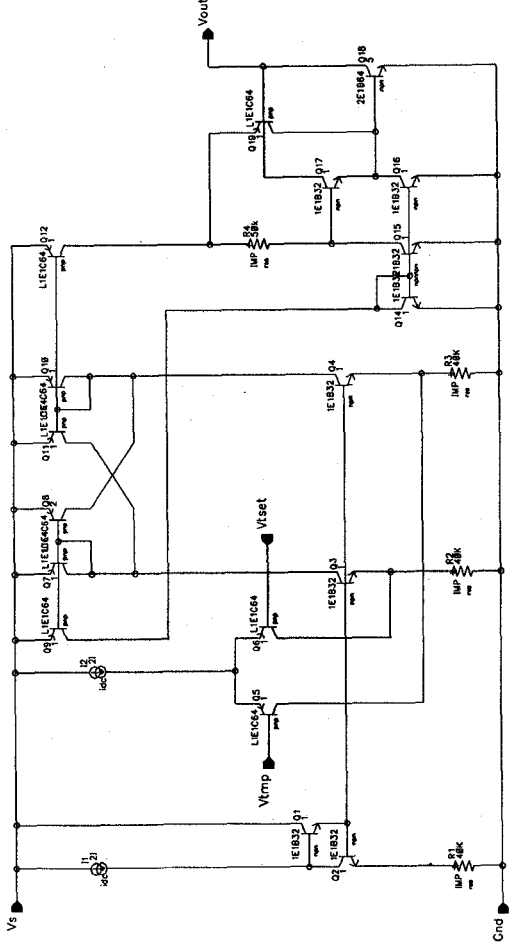

Figure 3a

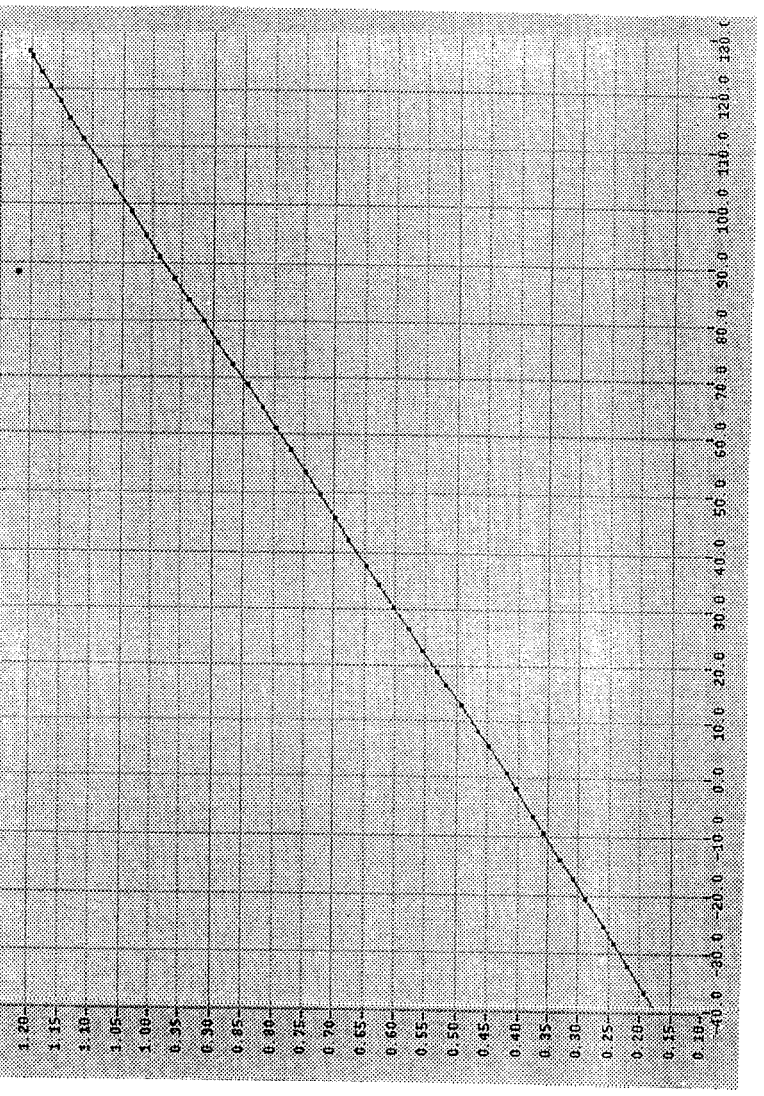

Figure 6

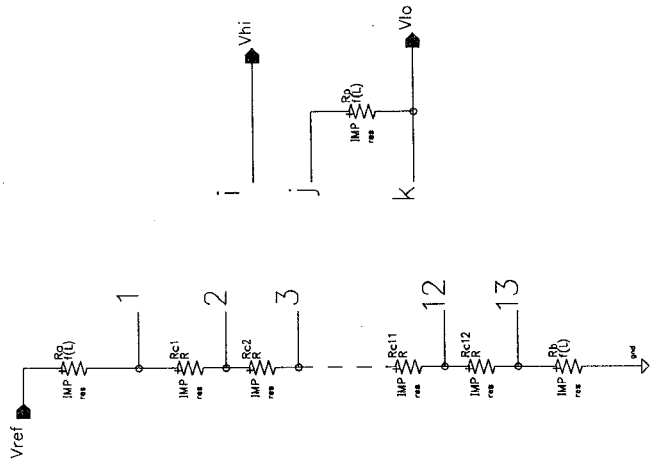

Figure 4

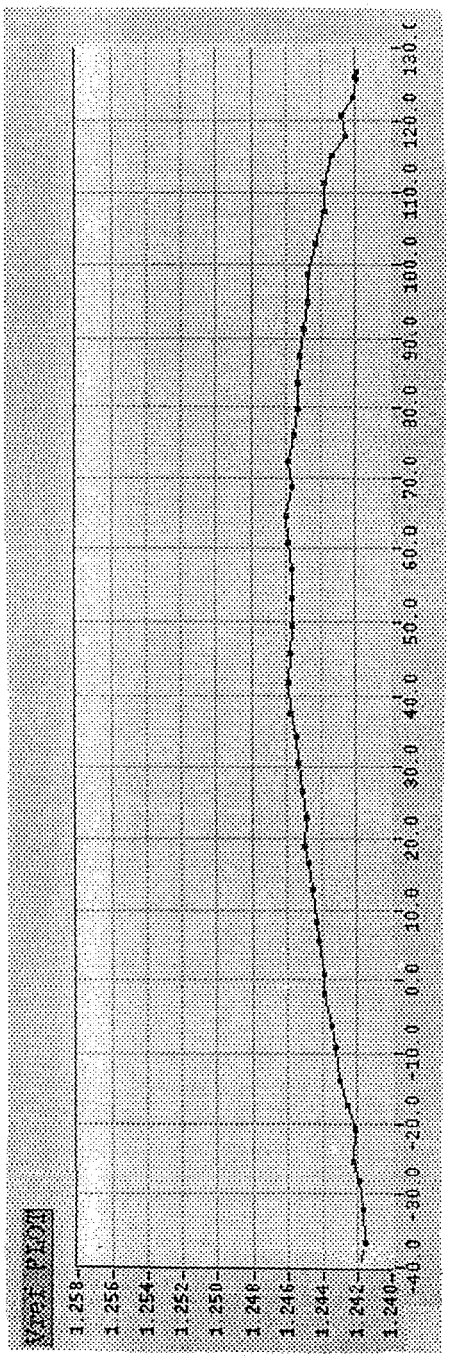

Figure 5