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POLYSILICON SOURCE DRAIN VMOST AND POLYSILICON SOURCE DRAIN GATE VMOST STRUCTURES

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Abstract - Two modified MOST structures called Polysilicon Source Drain VMOS Transistor (PSD-VMOST) and Polysilicon Source Drain Gate VMOS Transistor (PSDG-VMOST) obtained by the combination of PSD-MOST and Lateral VMOST technologies are suggested for a new work. The modification of PSD-MOST technology by V-groove technique brings all the advantages of Lateral VMOS and PSD-MOS Transistors to the new structure. Considerable decrease in the active area consumption and in the number of contact window improves the reliability of these structures.

I. INTRODUCTION

Recently, a new MOS Transistor (PSD-MOST) technology has been described [1]. The cross-section of a polysilicon source and drain MOST is given in Fig. 1. Polysilicon lines serve as a diffusion source as well as the conductive path to the source and drain. As a result, transistor and junction sizes are reduced by a factor 2 or 3 over a normal structure. The fabrication of the PSD-MOST requires 4 masks. Another recent development in the MOS technology is the Lateral VMOS Transistor [2] technology. The cross-section of a Lateral VMOST is given in Fig. 2. The fabrication involves either a 3 or 4 mask process and results in very short channel devices using non-critical alignment tolerances. The Lateral VMOST transistor exhibits lower output conductance and higher breakdown voltage than a standard MOS transistor. In this paper, two modified MOS structures called Polysilicon Source Drain VMOS Transistor (PSD-VMOST) and Polysilicon Source Drain Gate VMOS Transistor (PSDG-VMOST) obtained by the combination of (PSD-MOST) and (VMOST) technologies are suggested for a new work.

II. FABRICATION PROCEDURE

The fabrication technology for Polysilicon Source Drain VMOS Transistor involves five masking steps. The procedures are outlined in Fig. 3. For the purpose of illustration, n-type silicon (p-channel devices) will be considered; however, the processing steps would equally well apply to the fabrication of n-channel devices. A thick thermal oxide is first grown on the (100) orientation n-type silicon substrate. The first mask is used to determine the active area. A boron doped polysilicon layer is deposited on the slice. The second mask is used to define the polysilicon pattern. A thin oxide is grown on the slice. During this oxidation, the first drive-in occurs. A V-groove channel that separates the source and drain regions, is defined by unisotropically etching the silicon [3]. The depth of the groove depends on the width of the window opening. The gate oxide is thermally grown over the channel. The junction depth (therefore the channel length) is related to the second oxidation and the gate oxidation because drive-in and these oxidations take place simultaneously. The fourth mask is used to open contact windows. The fifth mask is used to define aluminum pattern.

The fabrication procedure for Polysilicon Source Drain Gate VMOS Transistor is outlined in Fig. 4. Until the gate oxidation, the procedure is similar to PSD-VMOST technology. After growing the gate oxide a boron doped polysilicon layer deposited on the slice. The thickness of this polysilicon layer must be sufficient to completely fill in the grooves. The front surface of the slice is then lapped flat, removing the polysilicon layer from all areas, except in the grooves [4 - 5] . The remaining steps are also similar to the PSD-VMOST technology. This structure results in flatter surface with less aluminum connections.

III. DISCUSSION

The characteristics of the PSD-VMOST at low values of drain-to-source voltage, is determined by the full channel, extending from the source to drain along the sloping walls of the groove. With increasing drain-to-source voltage (for a fixed gate-to-source voltage) the device enters the saturation region and channel pinch-off occurs initially at the bottom of the V-groove due to the thicker gate oxide present there, and the pinched-off region then extends from that point towards the drain diffusion, causing the effective channel length to be only half the geometrical channel length. The channel length modulation effects are reduced considerably, due to the pinch-off along the wall of the groove which takes up the excess drain voltage. Thus, the transistor exhibits very low values of source-drain output conductance in the saturation region. In PSD-MOST, the gate capacitances are relatively larger due to non-self-aligned gate structure [6] . In PSD-VMOST technology, by employing a thick field oxide, the gate overlap capacitances become dominated by the V-groove sidewall component which can be controlled by junction depth. Therefore, it is possible to fabricate transistors with low parasitic capacitances, and hence large cut-off frequencies. In PSD-VMOST, the diffused regions are always covered by a polysilicon layer. Therefore, it features two interconnect levels. Comparing to the standard process, the first level is lower ohmic which makes PSD-VMOST circuits less susceptible to wiring restrictions. The connection between the device and this first level is automatic, which leads to very small source and drain regions, hence to small devices. It is expected that this results in a shorter wiring, and therefore, in a higher packing density and circuit speed. The decrease in active area consumption and in the number of contact windows improves the reliability. It is expected that the PSDG-VMOS Transistor may exhibit all the advantages of a silicon gate MOSFET, notably: low threshold voltage, sealed-off gate oxide, and self-aligned gate.

IV. CONCLUSION

The modification of Polysilicon Source Drain MOST technology by V-groove technique, brings all the advantages of the Lateral VMOS and PSD-MOS transistors to the new structure. It is, therefore, expected that the new structure may result in relatively short channel lengths comparing to the standard MOST technology, high transconductance, small parasitic capacitances, high cut-off frequency, lower output conductance, considerably reduced area and metal connection lines. The decrease in active area consumption and in the number of contact windows improves the reliability of these structures. The suggested structures may be suitable to the fabrication of large scale integrated circuits for memory and logic applications, as well as linear MOS integrated circuits.

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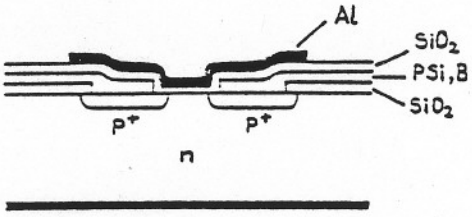

Fig. 1 PSD-MOST Structure

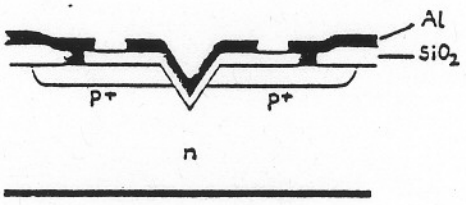

Fig. 2 Lateral VMOST Structure

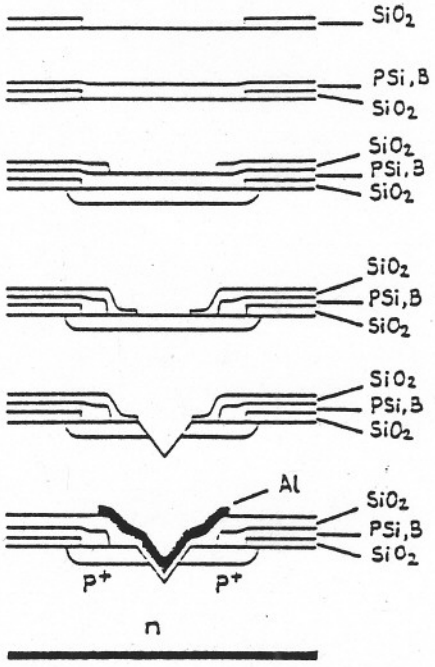

Fig. 3 PSD-VMOST Processing Steps

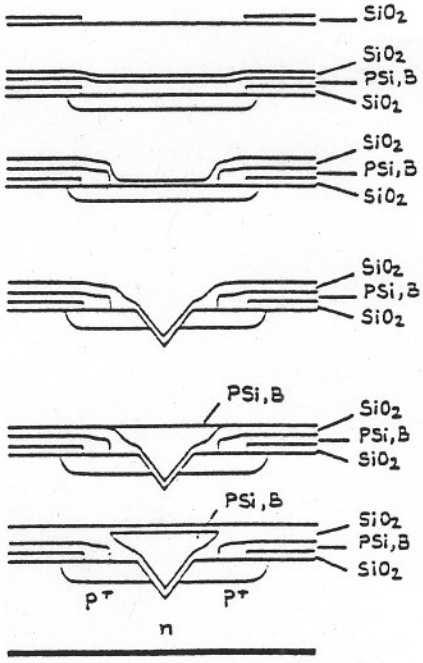

Fig. 4 PSDG-VMOST Processing Steps