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Modeling and simulation of an Analog Charge-Pump Phase Locked Loop

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ABSTRACT

We describe a nonlinear computer simulation model of an Analog Charge-Pump Phase Locked Loop (ACP-PLL). Offsets of the Phase Detector and Analog Charge-Pump are modeled as disturbances to simulate their effects on the steady-state phase error of the loop.

An extensive computer simulation study is carried out for the design of an example Analog CP-PLL using the proposed nonlinear model and comparing it to the conventional linear model. Results demonstrate the linear model is not sufficient to fully analyze and predict the behaviour of the Analog CP-PLL.

INTRODUCTION

The Analog CP-PLL is an electronic control system whose simplified block diagram is in Figure 1. The s_R and s_O are applied to the inputs of the Phase Detector which produces an output voltage s_D corresponding to the phase difference of these two input signals. The Phase Detector is followed by an Analog Charge-Pump. It consists of a Transconductance Amplifier with a capacitor at its output, forming an integrator. Note that this analog charge-pump is different from the Charge-Pump described by Gardner (1980) which is basically made of a current source/sink driven by a sequential-logic phase/frequency detector. The output of the loop filter is amplified and applied to the input of the Voltage Controlled Oscillator (VCO). This in turn produces an output signal at a frequency corresponding to the change of control voltage v_B such that it reduces the phase difference between s_R and s_O.

The operational characteristics of the Analog CP-PLL (Figure 1) are

(1) When the reference frequency f_R equals VCO frequency f_O, there is a 90° phase angle between s_R and s_O ($\Phi_E = \Phi_D - 90° = 0$).

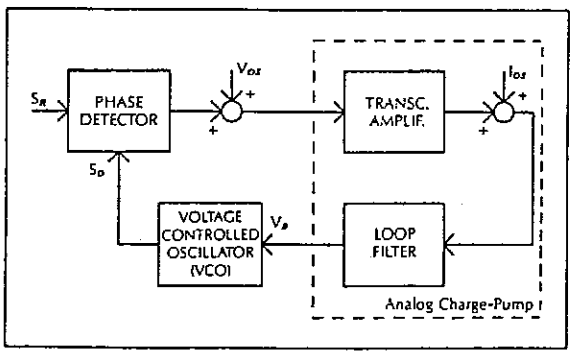

Figure 1. Analog Charge-Pump Phase Locked Loop (ACP-PLL).

(2) When the reference frequency changes to a new value, the VCO frequency takes up the same value within a required time interval, called "pull-in time" or "lock-in time." During this control action, the phase angle error ϕ_E, taken with respect to the 90° phase angle mentioned above, changes from zero to a positive or negative value and finally becomes zero when $f_R = f_O$ at the end of the pull-in time.

(3) When the reference frequency remains unchanged and a disturbance signal (i.e., V_{OS} and/or I_{OS}) enters into the system, the phase angle error changes from zero to a positive or negative value. The value of ϕ_E is proportional to the level of the offset signal.

The control action during the pull-in time is also known as the acquisition mode of operation. The control action, after frequency lock following a disturbance, is known as the tracking mode of operation. As in the following sections, all three major components of the Analog CP-PLL have nonlinearities.

Hence, the Analog CP-PLL is a nonlinear feedback control system whose system parameters and stability conditions which satisfy the prescribed performance requirements cannot be determined by well-known techniques such as "Root-Locus" and "Bode Plot" from the classical control theory. An efficient technique (Mitchell 1978; Dost and Liu 1985) to accomplish the task is use the power and flexibility of system simulation languages such as ACSL, CSSL-IV, or DSL/VS.

In this article, the usage of CSSL-IV is demonstrated in the determination of time-domain response characteristics of an example Analog CP-PLL.

The performance criteria of the Analog CP-PLL are set as:

(1) Settling time $< 2\ \mu s$

(2) Overshoot $< 20\%$

(3) Steady-state phase error $< 3°$

in response to the application of a 10% reference frequency step at $f_R = 10$ MHz; and Phase Detector offset $V_{OS} = 10$mV; and Charge-Pump offset $I_{OS} = 75\ \mu A$ in the form of step inputs.

MATHEMATICAL MODELING

Analog CP-PLL (see Figure 1) contains three main subcircuits: Phase Detector, Charge-Pump and Loop Filter, and Voltage Controlled Oscillator (VCO). We will briefly describe the operation of these subcircuits and present their mathematical models.

The main differences of this model from the classical models are that:

(1) The offsets of the Phase Detector and Charge-Pump are introduced into the model as disturbances.

(2) The Loop Filter is characterized with its state-space equations and used as a sub-block in the simulation.

Phase Detector: For a simplified circuit schematic of a typical analog phase detector see Figure 2. Apply the output of the VCO denoted by s_O to the upper transistor pairs Q3, Q4 and Q5, Q6. Apply the PLL's reference signal denoted by s_R to the lower transistor pair Q1, Q2. The input signals are given by:

$$s_R = A_R \sin(2\pi f_R t + \phi_R) \quad (1)$$

$$s_O = A_O \sin(2\pi f_O t + \phi_O) \quad (2)$$

where

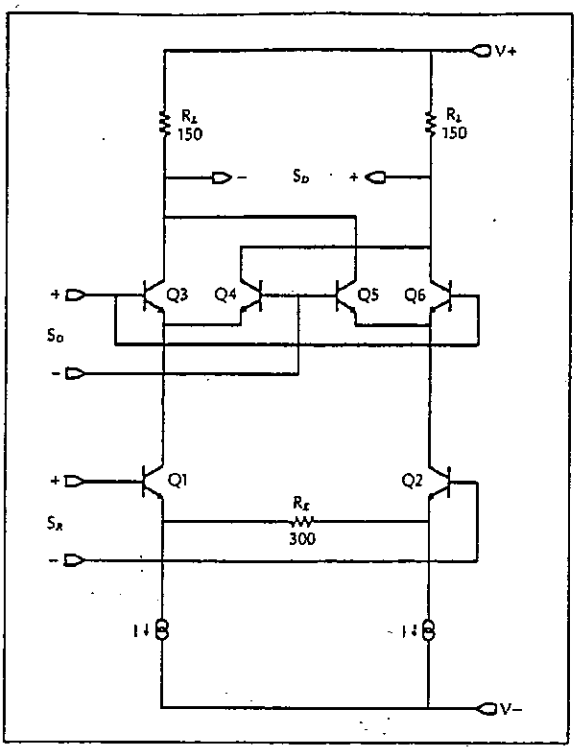

Figure 2. Simplified phase detector schematic.

A_R, A_O are the amplitudes; f_R, f_O are the frequencies and ϕ_R, ϕ_O are the phase angles of ACP-PLL's reference input and the VCO output, respectively.

An expression for the phase detector output signal S_D can be derived by observing its operational characteristics as follows:

- When s_R and s_O are in phase and have positive polarities, assume A_O is large enough so that transistors Q3, Q6 are fully turned "on" and transistors Q4, Q5 are fully turned "off." The differential pair Q1, Q2 and cascode transistors Q3, Q6 configuration yield a voltage of $s_D = (2R_L/R_E)s_R$ across load resistors R_L.
- When the input signals are in phase and have negative polarities, assume A_O is large enough so that transistors Q4, Q5 are fully turned "on" and transistors Q3, Q6 are fully turned "off." Since s_R is of negative polarity, differential pair Q1, Q2 and cascade transistors Q4, Q5 configuration yield a voltage of the same magnitude and polarity as in the previous case across load resistors R_L. Hence, the input reference signal is amplified. Also, its negative swinging half is inverted, producing an output signal s_D as a periodic function at twice the frequency of s_R with a maximum positive average dc level.
- When s_O lags s_R by 180°, using the same argument given above, s_D again is a similar periodic function with a maximum negative average dc level.
- When s_O lags s_R by 90°, s_D is a similar periodic function with a zero average dc level.
- When s_O lags s_R by any phase angle less than 90°, s_D is a periodic function with a positive average dc level. When s_O lags s_R by any phase angle more than 90°, s_D is a periodic function with a negative average dc level. In Figure 3 is the

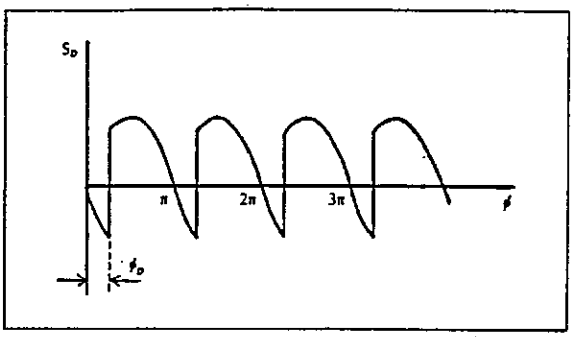

Figure 3. Phase detector output for a phase angle difference ϕ_D.

phase detector output signal s_D for a phase angle difference of ϕ_D between s_O and s_R.

Based on the above discussion an expression for s_D is given by:

$$s_D = (2R_L/R_E)\, s_R.\ \text{Sign}\,\{s_O\} \tag{3}$$

in which $(2R_L/R_E)$ is the dc gain of the phase detector, and Sign $\{s_O\}$ is defined by:

$$\text{Sign}\,\{s_O\} = +1 \qquad \text{for } s_O > 0 \tag{4a}$$

$$\text{Sign}\,\{s_O\} = 0 \qquad \text{for } s_O = 0 \tag{4b}$$

$$\text{Sign}\,\{s_O\} = -1 \qquad \text{for } s_O < 0 \tag{4c}$$

From Figure 3, an average value of s_D is given by:

$$s_D = (2R_L/\pi R_E)^*(\int_{t_o}^{\pi} A_R \sin\varphi\, d\varphi\ - \int_0^{t_o} A_R \sin\varphi\, d\varphi) \tag{5}$$

carrying out the integration in Eq. 5 yields:

$$s_D = (4R_L A_R/\pi R_E)\ \text{Cos}\tfrac{1}{2}\phi_D \tag{6}$$

Since $\frac{1}{2}\phi_E = \frac{1}{2}\phi_D - 90°$, Eq. 6 can be rewritten as:

$$s_D = (4R_L A_R/\pi R_E)\ \text{Sin}\tfrac{1}{2}\phi_E \tag{7}$$

Charge-Pump and Loop Filter: A simplified circuit schematic of an Analog Charge-Pump is in Figure 4. The differential output of the phase detector is applied to the input of differential pair Q1, Q2. The output current I_{CP} of this transconductance amplifier charges and discharges the capacitor C_{CP}. For $R_{CP} = 0$, the output current of the charge-pump is given by:

$$I_{CP} = I_{CS}\ \text{Tanh}\,(s_D/V_T) \tag{8}$$

where

I_{CS} is the constant current source; V_T is given by kT/q in which k is the Boltzmann constant, T is the absolute temperature, and q is the electronic charge. When $R_{CP} \neq 0$, the expression given in Eq. 8 can be simplified to a linear relationship as:

$$I_{CP} = (1/R_{CP})\ s_D \tag{9}$$

The Loop Filter forms by series connection of a resistor R_X and

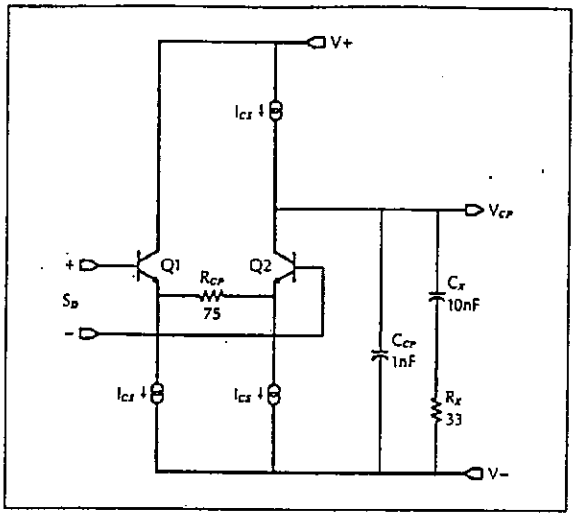

Figure 4. Simplified schematic of the Analog Charge-Pump and Loop Filter.

a capacitor C_X. The state equations for the configuration in Figure 4 are given by:

$$\dot{v}_{CP} = -[(b-1)/\tau]\, v_{CP} + [(b-1/\tau]\, v_{CX} + [(b-1)/C_X]\, I_{CP} \tag{10}$$

$$\dot{v}_{CX} = (1/\tau)\, v_{CP} - (1/\tau)\, v_{CX} \tag{11}$$

where

$\tau = R_X C_X$; $b = 1 + C_X/C_{CP}$.

Voltage Controlled Oscillator: A negative resistance LC type oscillator is considered as a VCO in this article. A simplified schematic of such oscillator is in Figure 5. The differential pair Q1, Q2 which is connected in a positive feedback configuration forms a negative resistor. The combination of an inductor L, a capacitor C_V and the negative resistor produces the oscillations at the collector of Q1. The amplitude of the oscillations is controlled by a subcircuit which varies the negative resistor by changing the tail current of differential pair Q1, Q2. The amplifier A drives a frequency divider circuit. The frequency of oscillation is given by:

$$f_O = K_D/2\pi[L\ C_V(v_B)]^{1/2} \tag{12}$$

where

K_D is coefficient introduced by the frequency divider ($K_D = 1/2$) circuit which follows the VCO and v_B is the output voltage of the buffer/amplifier following the charge-pump and is given by:

$$v_B = K_B\ v_{CP} \tag{13}$$

A voltage controlled capacitor (varactor) is used to realize frequency control by voltage. The capacitance C_V versus the buffer voltage v_B characteristic is nonlinear. However, the f_O versus v_B characteristic for a particular varactor used in our example is almost linear. Hence, Eq. 12 can be linearized and re-written as:

$$f_O = K_O\ v_B + f_{OC} \tag{14}$$

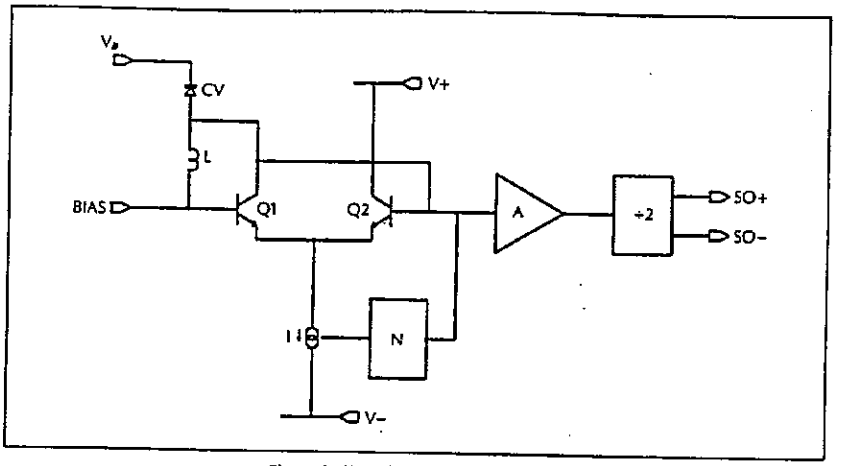

Figure 5. Simplified schematic of VCO.

where f_{OC} is the VCO's frequency of oscillation at $v_B = 0$, which is called center frequency (or free running frequency). Equation 14 is used in the linear analysis part of this study. The output of the VCO is given by:

$$s_O = A_O \sin[2\pi f_O(v_B)t + \phi_O(v_B)] \tag{15}$$

where

$$\dot{\phi}_O = f_O(v_B) \tag{16}$$

In Figure 6 is the complete block diagram corresponding to the nonlinear mathematical model developed for the Analog CP-PLL. Note that the offset voltage of the phase detector v_{OS} and the offset current of the charge-pump i_{OS} are introduced as disturbance signals in Figure 6.

COMPUTER SIMULATION

A computer simulation of the proposed Analog CP-PLL model is carried out in the following steps:

Step1. *Linear Analysis.* For small changes of ϕ_E, $\sin\phi_E$ is approximately equal to ϕ_E. Therefore, Eq. 7 can be linearized as:

$$s_D = (4R_L A_R/\pi R_E)\phi_E \tag{17}$$

Using linearized models of phase detector, transconductance amplifier and VCO given by Eqs. 17, 9, and 14 respectively, we obtain the block diagram of the linearized ACP-PLL as in Figure 7.

When the phase detector and charge-pump offsets are introduced into the system as $v_{OS} = v_{OS}\,u(t)$ and, $i_{OS} = I_{OS}\,u(t)$ where $u(t)$ being a unit step function, from the block diagram in Fig-

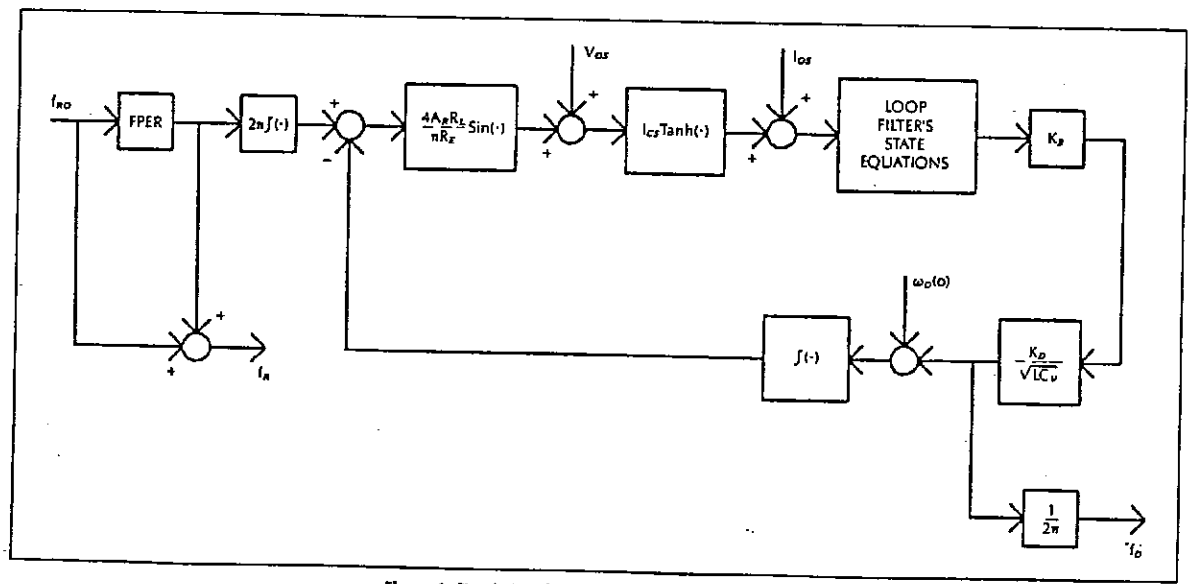

Figure 6. Simulation diagram of the nonlinear ACP-PLL.

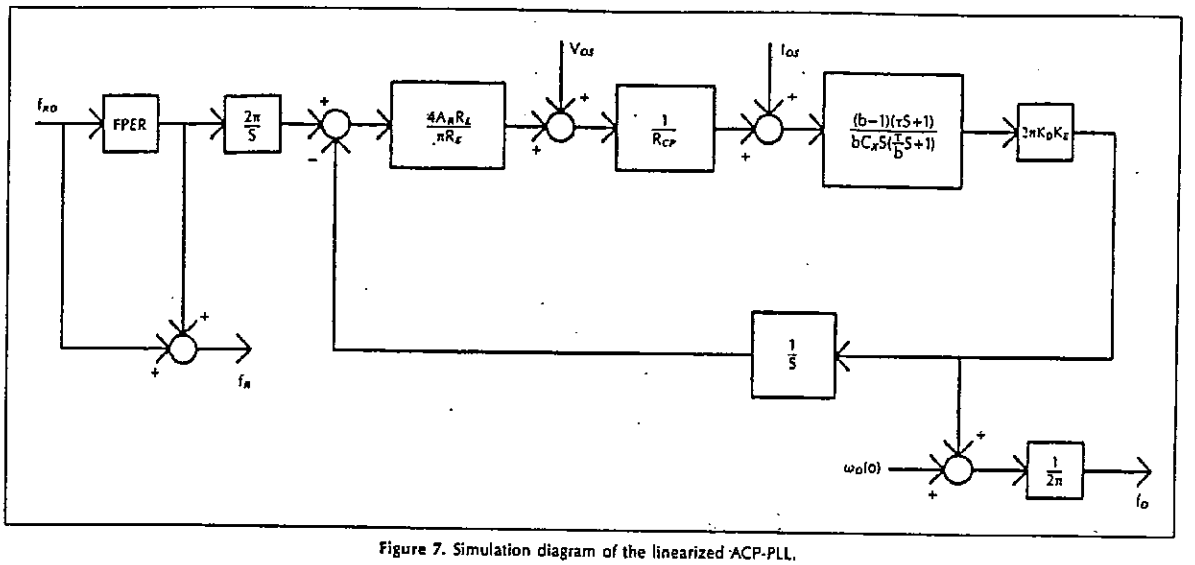

Figure 7. Simulation diagram of the linearized ACP-PLL.

ure 7, it can be shown that the steady-state phase error (Gardner 1979) due to offsets is:

$$\bar{\phi}_e = (\pi R_E/4A_R R_L)[V_{OS} + R_{CP} I_{OS}] \quad (18)$$

From Figure 7, the closed-loop transfer function (when offsets are zero) is obtained as:

$$\bar{\phi}_O/\bar{\phi}_R = F(s)/[1 + F(s)] \quad (19)$$

where

$$F(s) = K(s + 1/\tau)/[s^2(s + b/\tau)] \quad (20)$$

in which

$$K = [8R_L A_R (b - 1) K_B K_O]/[R_E R_{CP} C_X] \quad (21)$$

$$\tau = R_X C_X \quad (22)$$

Substituting Eq. 20 into Eq. 19 we obtain:

$$\bar{\phi}_O(s)/\bar{\phi}_R(s) = K(s + \tau)/[s^3 + (b/\tau)s^2 + Ks + (K/\tau)] \quad (23)$$

where the characteristic equation is:

$$s^3 + (b/\tau)s^3 + Ks + (K/\tau) = 0 \quad (24)$$

The roots of Eq. 24 determine the response characteristics of the linear system as in Figure 7. Here, the system parameters used are $A_R = 0.2V$; $K_B = 2$; $K_O = 3.67 * 10^6$ Hz/V; $C_X = 10nF$; $R_X = 33$ ohm; $b = 11$; $R_L = 150$ ohm; $R_E = 300$ ohm. From the Root Locus diagram (not shown here) of Eq. 24, the roots of the characteristic equation and the gain which yield an acceptable system performance are determined. As a result, an initial value of 150 ohm is selected for the resistor, R_{CP}, of the linearized charge-pump.

A computer simulation program using CSSL-IV was developed (Can and Sahinkaya 1986) for the linear ACP-PLL and simulated for a 10% frequency step (i.e., *FPER* = 0.1) and zero offsets. The ACP-PLL response is in Figure 8a.

Step2. *Nonlinear Analysis.* A CSSL-IV program is also developed (Can and Sahinkaya 1986) for the nonlinear ACP-PLL model of Figure 6. The response of the nonlinear ACP-PLL for a same input frequency step as in linear ACP-PLL is in Figure 8b. From Figure 8, the following conclusions are drawn:

(1) The linear model *is not adequate* for predicting the response characteristics of the ACP-PLL.

(2) The "pull-in time" as predicted by the nonlinear model, with previously assumed circuit parameters, is about 14 μs which is about twice the value obtained from the linear model, and seven times larger than the maximum allowable value of 2 μs. Note that here, $R_{CP} = 150$ ohms. To reduce the "pull-in time" to an acceptable value, the loop gain must be increased without exceeding the stability limit. At this point, for the design method used in choosing the parameter values one may refer to a recent article by Gardner (1980).

Several computer runs have been made to optimize the design. Only the most interesting results are given here. The VCO frequency (see Figure 8b) loses its synchronism with the reference frequency for about 4 cycles before a "lock-in" is achieved. This clearly demonstrates the importance of the nonlinear analysis since the linear model will not show such characteristics. In Figure 9 is the response for final selection of parameter R_{CP} as 75 ohms for a frequency step of 10%.

In Figure 10 is the step response of the ACP-PLL when the linearized charge-pump model is replaced with the nonlinear model and other parameters are kept the same as in Figure 9. With the nonlinear charge-pump, the "lock-in" time is further reduced from approximately 5 μs (see Figure 9) to less than 2 μs.

CONCLUSIONS

A nonlinear mathematical model is developed for the simulation of Analog Charge-Pump Phase Locked Loops. Using CSSL-

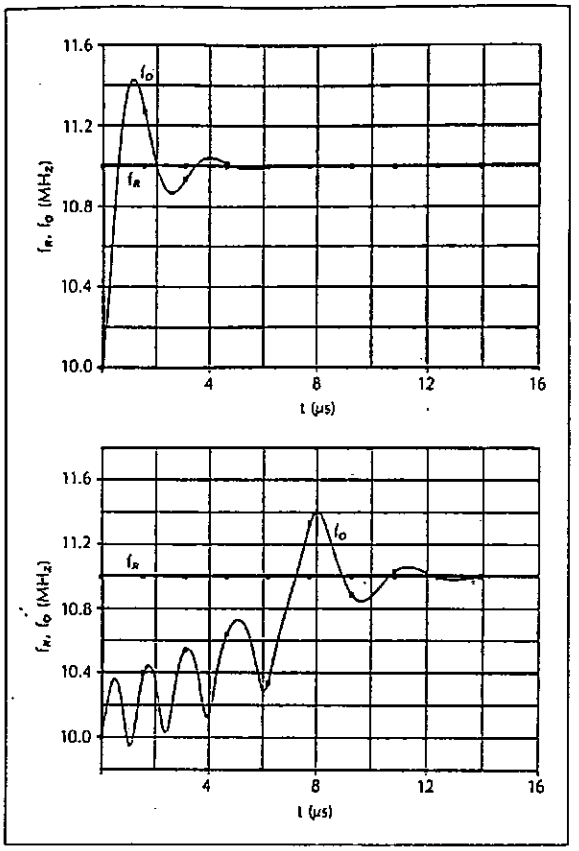

Figure 8. Step input response of (a) the linear ACP-PLL (R_{CP}=150Ω) (b) the nonlinear ACP-PLL with linear charge-pump (R_{CP}=150Ω).

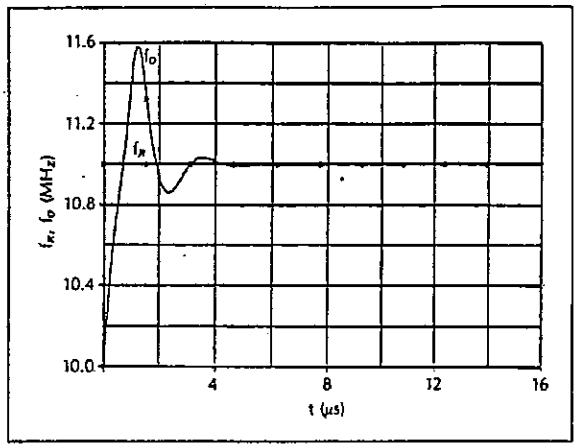

Figure 9. Step input response on nonlinear ACP-PLL with linear charge-pump (R_{CP}=75 ohms).

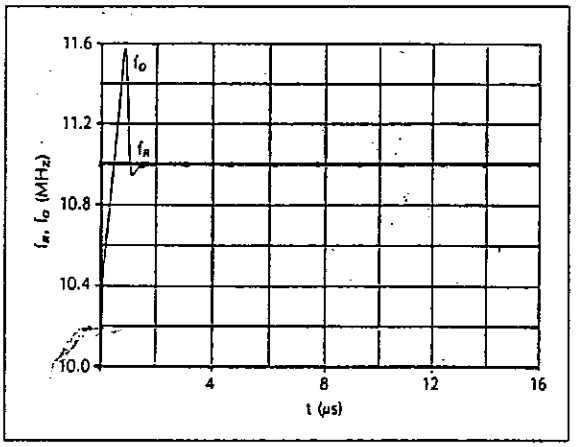

Figure 10. Step input response of nonlinear ACP-PLL with nonlinear charge-pump (R_{CP}=0).

IV, it was once again clearly shown that the linearized model is not sufficient to fully analyze and predict the response characteristics of the loop. It is almost mandatory to use computer based nonlinear analysis methodology for the design of Analog Charge-Pump Phase Locked Loops. The Phase Detector and Charge-Pump offsets are introduced as disturbances into the model and their influence on the ACP-PLL response characteristics is investigated.

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