A computer simulation model for an analog charge-pump phase locked loop

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ABSTRACT

A nonlinear computer simulation model of an Analog Charge-Pump Phase Locked Loop (CP-PLL) is described in this paper. Off-sets of the Phase Detector and analog Charge-Pump are modeled as disturbances in order to simulate their effects on the steady-state phase error of the loop.

Extensive computer simulation study is carried out for the design of an example Analog CP-PLL using the proposed nonlinear model and compared to the conventional linear model. The simulation results clearly demonstrate that the linear model is not sufficient to fully analyse and predict the behaviour of the Analog CP-PLL.

INTRODUCTION

The Analog CP-PLL [1] is an electronic control system whose simplified block diagram is shown in Fig.1 . The s_R and s_0 are applied to the inputs of the Phase Detector which produces an output voltage s_D corresponding to the phase difference of these two input signals. The Phase Detector is followed by a Charge Pump consisting of a Transconductance Amplifier with a capacitor at its output, forming an integrator ,and a Loop Filter. The output of the Charge Pump is amplified and applied to the input of the Voltage Controlled Oscillator (VCO) which produces an output signal at a frequency corresponding to the change of control voltage v_R in such a way that it reduces the phase difference between s_R and s_0 .

The operational characteristics of the Analog CP-PLL shown in Fig.1 are as follows:

1. When the reference frequency f_R is equal to VCO frequency f_0 , there is a 90 degree phase angle between s_R and s_0 . If , Phase Detector offset V_{os} = 0 , and the Charge Pump offset I_{os} = 0 , then the Phase Detector output s_D = 0 . When this happens , v_R has a steady state value because of the integrator action on the error signal .

2. When the reference frequency changes to a new value , the VCO frequency takes up the same value within a required time interval which is called "pull-in time" or "lock-in time" . During this control action , the phase angle error ϕ_E ,which is taken with respect to 90 degree phase angle mentioned above , changes from zero to a positive or negative value and finally becomes zero when $f_R = f_0$ at the end of the pull-in time.

3 When the reference frequency remains unchanged and a disturbance signal (i.e. V_{os} and/or I_{os}) enters into the system , the phase angle error changes from zero to a positive or negative value when $f_R = f_0$ at the end of the pull-in time . The value of ϕ_E is proportional to the level of the offset signal.

The control action during the pull-in time is also known as the "acquisition mode of operation" .The control action after frequency lock following a disturbance of the form mentioned in 2 and 3 is known as the "tracking mode of operation" . As shown in the following sections , all three major components of the Analog CP-PLL have nonlinearities.

Hence , the Analog CP-PLL is a nonlinear feedback control system whose system parameters and stability conditions that satisfy the prescribed performance requirements can not be determined by well-known techniques such as "Root-Locus" , "Bode Plot" from the classical control theory. An efficient technique [2-3] in accomplishing ,the above task is to utilize the power and flexibility of proven system simulation languages such as ACSL [4] , CSSL-IV [5] , or DSL/VS [6] .

In this article , the usage of CSSL-IV is demonstrated in the determination of time-domain response characteristics of an example Analog CP-PLL in response to prescribed disturbances.

The performance criteria of the Analog CP-PLL is set as in the following:

1. Settling Time < 2 microseconds

2. Overshoot < 20%

3. Steady State Phase Error < 3 degrees

in response to the application of a 10% reference frequency step at f_R =10 MHz , and Phase Detector offset V_{os} = 10mV and Charge Pump offset I_{os} =75 μA in the form of step inputs.

MATHEMATICAL MODELING

Analog CP-PLL shown in Fig.1 contains three main subcircuits which are; 1.Phase Detector, 2.Charge Pump and Loop Filter, 3.Voltage Controlled Oscillator. The operation of these subcircuits are briefly described and their mathematical models are presented in this section.

1.Phase Detector : A simplified circuit schematic of a typical analog phase detector is shown in Fig 2 . The output of the VCO denoted by s_0 is applied to the upper transistor pairs Q3,Q4 and Q5,Q6 while the PLL's reference signal denoted by s_R is applied to the lower transistor pair Q1,Q2. The input signals are given by

$$s_R = A_R \sin(2\pi f_R t + \phi_R) \qquad (1)$$

$$s_R = A_R \sin(2\pi f_R t + \phi_R) \qquad (2)$$

where A_R , A_0 are the amplitudes ; f_R , f_0 are the frequencies and ϕ_R , ϕ_0 are the phase angles of CP-PLL's reference input and the VCO output respectively .

An expression for the phase detector output signal s_D can be derived by observing its operational characteristics as in the following:

*When s_R and s_0 are in phase and have positive polarities ; Assume A_0 is large enough so that transistors Q3 , Q6 are fully turned "on" and transistors Q4 , Q5 are fully turned "off" . The differential pair Q1,Q2 and cascode transistors Q3,Q6 configuration yields a voltage of $s_D=(2R_L/R_E)s_R$ across load resistors R_L .

*When the input signals are in phase and have negative polarities; Assume A_0 is large enough so that transistors Q4,Q5 are fully turned "on" and transistors Q3,Q6 are fully turned "off" . Since s_R is of negative polarity , differential pair Q1,Q2 and cascade transistors Q4,Q5 configuration yields a voltage of same magnitude and polarity as previous case across load resistors R_L . Hence when the phase error $\phi_D=0$, the input reference signal is amplified and also its negative swinging half is inverted , producing an output signal s_D as a periodic function at twice the frequency of s_R with a maximum positive average dc level.

*When s_0 lags s_R by 180 degrees ,using the same argument given above it can be shown that s_D is again a similar periodic function with a maximum negative average dc level.

*When s_0 lags s_R by 90 degrees , s_D is a similar periodic function with a zero avarage dc level.

*When s_0 lags s_R by any phase angle less than 90 degrees , s_D is a periodic function with a positive avarage dc level. When s_0 lags s_R by any phase angle more than 90 degrees , s_D is a periodic function with negative avarage dc level. Fig.3 shows the phase detector output signal s_D versus phase angle ϕ_E characteristic.

Based on the above discussion an expression for s_D is given by;

$$s_D=(2R_L/R_E)s_R \cdot \mathrm{Sign}\{s_0\} \qquad (3)$$

in which $(2R_L/R_E)$ is the dc gain of the phase detector , and $\mathrm{Sign}\{s_0\}$ is defined by;

$$\mathrm{Sign}\{s_0\} = +1 \quad \text{for } s_0 > 0 \qquad (4a)$$
$$\mathrm{Sign}\{s_0\} = 0 \quad \text{for } s_0 = 0 \qquad (4b)$$
$$\mathrm{Sign}\{s_0\} = -1 \quad \text{for } s_0 < 0 \qquad (4c)$$

Fig.4 shows the phase detector output signal s_D versus phase angle error ϕ_E over the region $-\pi < \phi_E < \pi$ where;

$$\phi_D = \phi_E - 90^\circ \qquad (5)$$

From Fig.4 , an avarage value of s_D is given by ;

$$s_D=(2R_L/R_E)\cdot\left(\int_{\phi_D}^{\pi} A_R \sin\varphi \, d\varphi - \int_{0}^{\phi_D} A_R \sin\varphi \, d\varphi\right) \qquad (6)$$

carrying out the integration in Eqn.6 yields ;

$$s_D = (4R_L A_R/\pi R_E)\cos\phi_D \qquad (7)$$

Using the definition given in Eqn.5 , equation (7) can be re-written as;

$$s_D = (4R_L A_R/\pi R_E)\sin\phi \qquad (8)$$

2.Charge Pump and Loop Filter : Simplified circuit schematic of an Analog Charge Pump is shown in Fig.5 . The differential output of the phase detector is applied to the input of differential pair Q1,Q2 . The output current I_{CP} of this transconductance amplifier charges and discharges the capacitor C_{CP} . For $R_{CP}=0$, the output current of the charge pump is given by ;

$$I_{CP} = I_{CS} \tanh(s_D/V_T) \qquad (9)$$

where I_{CS} is the constant current source and V_T is given by kT/q in which k is the Boltzman constant, T is the absolute temperature and q is the electronic charge . When $R_{CP}\neq 0$, the expression given in Eqn.9 can be simplified to a linear relationship as ;

$$I_{CP} = (1/R_{CP})\, s_D \qquad (10)$$

The Loop Filter is formed by series connection of a resistor R_X and a capacitor C_X . The state equations for the configuration shown in Fig 6 is given by;

$$\dot{v}_{CP}=-[(b-1)/\tau]v_{CP}+[(b-1)/\tau]v_{CX}+[(b-1)/C_X]I_{CP} \qquad (11)$$

$$\dot{v}_{CX} = (1/\tau)v_{CP} - (1/\tau)v_{CX} \qquad (12)$$

where $\tau = R_X C_X$ and $b = 1 + C_X/C_{CP}$.

3.Voltage Controlled Oscillator : A negative resistance LC type oscillator [7] is considered as a VCO in this article . A simplified schematic of such oscillator is shown in Fig.7 . The differential pair Q1 ,Q2 which is connected in a positive feedback configuration forms a negative resistor. The combination of an inductor L , a capacitor C_V and the negative resistor produces the oscillations at the collector of Q1 . The amplitude of the oscillations are controlled by a subcircuit which varies the negative resistor by changing the tail current of differential pair Q1,Q2. The amplifier A drives a frequency divider circuit. The frequency of oscillation is given by;

$$f_0 = K_D/2\pi[L\, C_V(v_B)]^{1/2} \qquad (13)$$

where K_D is coefficient introduced by the frequency divider ($K_D=1/2$) circuit which follows the VCO and v_B is the output voltage of the buffer/amplifier following the charge pump and is given by;

$$v_B = K_B\, v_{CP} \qquad (14)$$

A voltage controlled capacitor (varactor) [8] is used to realize frequency control by voltage . The capacitance C_V versus the buffer voltage v_B

characteristic is nonlinear. However , f_0 versus v_B characteristic with this particular varactor is almost linear. Hence , Eqn.13 can be linearized and re-written as ;

$$f_0 = K_0 v_B + f_{0C} \qquad (15)$$

where f_{0C} is the VCO's frequency of oscillation at $v_B = 0$, which is called center frequency (or free running frequency). Eqn.15 is used in the linear analysis part of this study. The output of the VCO is given by;

$$s_0 = A_0 \sin[2\pi f_0(v_B)t + \phi_0(v_B)] \qquad (16)$$

where,

$$\phi_0 = f_0(v_B) \qquad (17)$$

Fig.8 shows the complete block diagram corresponding to the nonlinear mathematical model developed for the Analog CP-PLL . It should be noted that the offset voltage of the phase detector v_{0S} and the offset current of the charge pump i_{0S} are introduced as disturbance signals in Fig.8 .

COMPUTER SIMULATION

A computer simulation of the proposed Analog CP-PLL model is carried out in the following steps:

Step1.Linear Analysis: For small changes of ϕ_E , $\sin\phi_E$ is approximately equal to ϕ_E .Therefore , Eqn.8 can be linearized as ;

$$s_0 = (4R_L A_B' / \pi R_E)\ \phi_E \qquad (18)$$

Using linearized models of phase detector , transconductance amplifier and VCO given by equations (18) , (10) and (15) respectively, we obtain the block diagram of linearized CP-PLL as shown in Fig.9 .

When the phase detector and charge pump offsets are introduced into the system as $v_{0S} = V_{0S}\ u(t)$ and, $i_{0S} = I_{0S}\ u(t)$ where $u(t)$ being a unit step function ; from the block diagram in Fig.9 , it can be shown that the steady state phase error [9] due to offsets is;

$$\phi_e = (\pi R_E / 4A_B R_L)\ [V_{0S} + R_{CP}\ I_{0S}] \qquad (19)$$

From Fig.9 , the closed-loop transfer function (when offsets are zero) is obtained as

$$\phi_0/\phi_R = F(s) / [1 + F(s)] \qquad (20)$$

where

$$F(s) = K\ (s+1/\tau) / [s^2\ (s+b/\tau \qquad (21)$$

in which

$$K = [8R_L A_B (b-1) K_B K_0] / [R_E R_{CP} C_I] \qquad (22)$$

$$\tau = R_I C_I \qquad (23)$$

Substituting Eqn.21 into Eqn.20 we obtain ;

$$\phi_0(s)/\phi_R(s) = K(s+I)/[s^3 + (b/\tau)s^2 + Ks + (K/\tau)] \qquad (24)$$

where the characteristic equation is ;

$$s^3 + (b/\tau)s^2 + Ks + (K/\tau) = 0 \qquad (25)$$

The roots of Eqn.25 determines the response characteristics of the linear system shown in Fig.9 . Here , the following system parameters are used; $A_B = 0.2$ V, $K_B = 2$, $K_0 = 3\ 67 * 10^8$ Hz/V , $C_I = 10$nF , $R_I = 33$ ohm , $b=11$, $R_L = 150$ ohm , $R_E = 300$ ohm . From the Root Locus [10] diagram (not shown here) of Eqn.25 , the roots of the characteristic equation , and the gain which yield an acceptable system performance , are determined. As a result , an initial value of 150 ohm is selected for the resistor of the linearized charge pump.

A computer simulation program using CSSL-IV [5] is written for the linear CP-PLL. Using the program shown in Fig.10a , the linear CP-PLL is simulated for a 10% frequency step (i.e. FPER=0.1) and zero offsets. The CP-PLL response is shown in Fig.11a .

Step2.Nonlinear Analysis: The CSSL-IV program developed for nonlinear CP-PLL model of Fig.8 is shown in Fig.10b . The response of the nonlinear CP-PLL for a same input frequency step as in linear CP-PLL is shown in Fig.11b . From Fig.11 ,the following conclusions are drawn:

1. The linear model is not adequate for predicting the response characteristics of the CP-PLL.
2.The "pull-in time" as predicted by nonlinear model with previously assumed circuit parameters is about 14 microseconds which is about twice the value obtained from linear model , and seven times larger than the maximum allowable value of 2 microseconds. Note that here ; $R_{CP} = 150$ ohms. In order to reduce the "pull-in time" to an acceptable value , it is known from control theory that the loop gain must be increased without exceeding the stability limit. Several computer runs have been made to optimize the design . Only the most interesting results are given below. Fig.11b shows that the VCO frequency loses its synchronism with the reference frequency for about 4 cycles before a "lock-in" is achieved. This clearly demonstrates the importance of the nonlinear analysis since the linear model wil not show such characteristics . Fig.12 shows the response for final selection of parameter R_{CP} as 75 ohms and a frequency step of 10%.

Fig.13 shows the step response of the CP-PLL when the linearized charge pump model is replaced with nonlinear model and other parameters kept the same as in Fig.12 . With the nonlinear charge pump , the "lock-in" time reduced from approximately 5 microseconds (see Fig.12) to less than 2 microseconds.

Fig.14a shows the response characteristics of the CP-PLL for a phase detector offset of $V_{0S} = 10$mV while FPER=0 and $I_{0S} = 0$. Fig.14b shows the same characteristic for a charge pump offset of $I_{0S} = 75\ \mu$A while $V_{0S} = 0$. The system response characteristics are stable and performance criteria such as: pull-in time $< 2\ \mu$sec and phase error $< 3°$ are satisfied.

CONCLUSIONS

A nonlinear mathematical model is developed for the simulation of Analog Charge Pump Phase Locked Loops. It was clearly demonstrated that the linearized model is not sufficient to fully analyse and predict

the response characteristics of the loop. It is almost mandatory to use a proven computer based nonlinear analysis methodology for the design of Analog Charge Pump Phase Locked Loops. The Phase Detector and Charge Pump offsets are introduced as disturbances into the model and their influence on the CP-PLL response characteristics is demonstrated.

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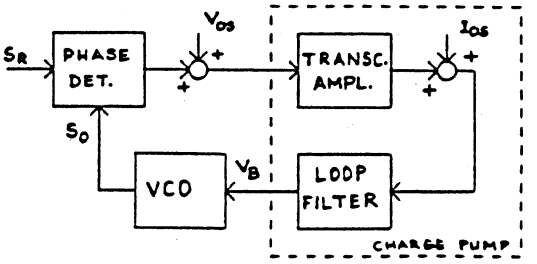


Fig.1: Analog Charge Pump Phase Locked Loop

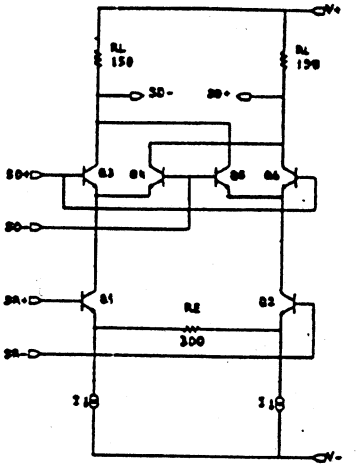


Fig.2 : Simplified Phase Detector Schematic

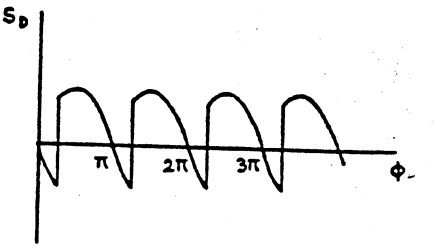


Fig.3 : Phase Detector Output s_D versus Phase Angle ϕ_E

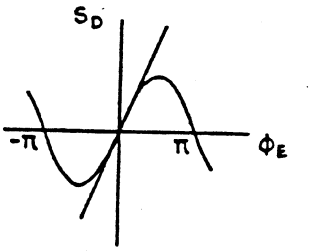


Fig.4 : Phase Detector Output s_D versus Phase Angle ϕ_E

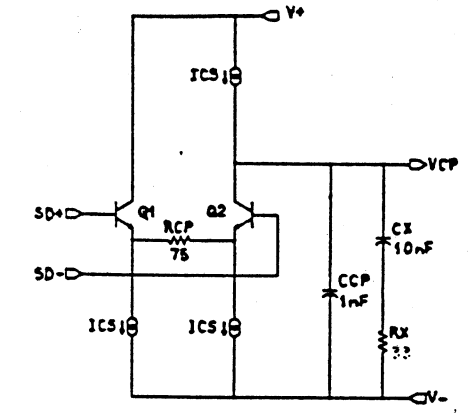


Fig.5 : Simplified Schematic of Charge Pump and Loop Filter

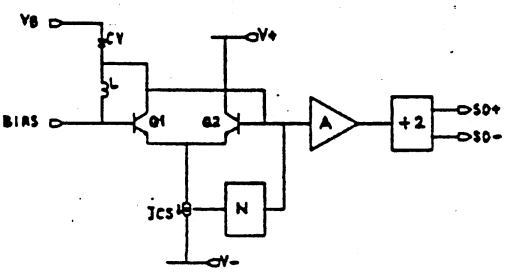
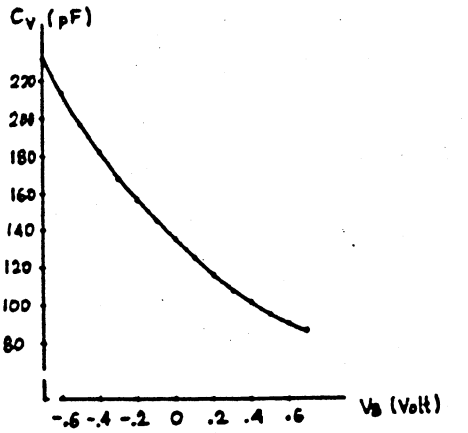


Fig.6 : Simplified Schematic of the Voltage Controlled Oscillator andFrequency Divider



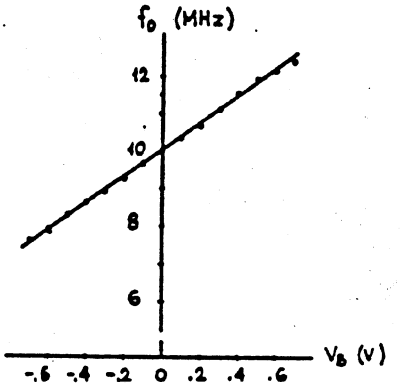


Fig.7 : a)Voltage Controlled Capacitor Characteristic b)VCO Frequency versus Control Voltage

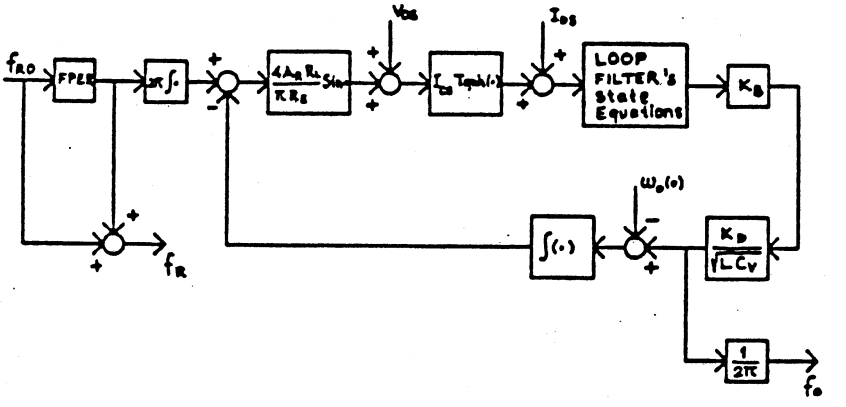


Fig.8 : Simulation Diagram of the Nonlinear Analog CP-PLL

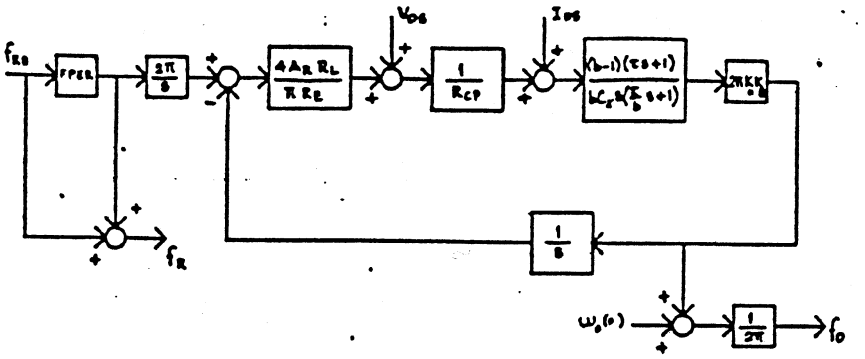
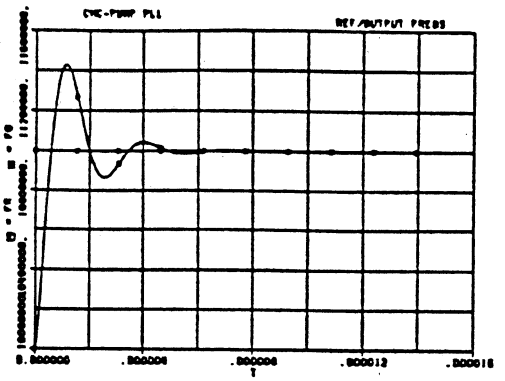


Fig.9 : Simulation Diagram of the Linearized CP-PLL

```
* LINEAR MODEL *
* THIS IS A CHARGE PUMP PHASE LOCK LOOP MODEL *
*TRANSIENT RESPONSE ANALYSIS*
* SYSTEM PARAMETERS *
CONSTANT PI=3.14144.AP= 0.2.RCP=150.0.R1=33.0....
         C1=10.0E-9.CCP=1.0E-9
CONSTANT AMP=1.0.TFIN=15.0E-6.TSTART=0.0
CONSTANT VPO=0.0.VCPO=0.0.PHIRO=0.0.PHIDO=0.0
CONSTANT KD=5.27E+6.KO=2.0
CONSTANT VOFF=0.0.IOFF=0.0.FRO=10.0E+6....
         FPER=0.10.CVO=138.0E-12....
    FVCDO=20.0E+6.CVC=1.0E-12.FDR=2.0
* VARACTOR CAPACITANCE VERSUS VOLTAGE-VB *
TABLE CVT.1.17.-0.7.-0.7.-0.6.-0.5.-0.4.-0.3.-0.2.-0.1....
              0.0.0.1.0.2.0.3.0.4.0.5.0.6.0.7.0.7....
              232.0.232.0.214.0.197.0.182.0.169.0.157.0....
            148.0.138.0.128.0.117.0.109.0.101.0.95.0....
            90.0.87.0.87.0
INITIAL
B=1.0+(C1/CCP)
TAU2=(R1+C1)
TLEAD=TAU2
TLAG=(TAU2/B)
CV=CV0
FVCO=FVCDO
LV=(1.0/(CV0+(2.0*PI*FVCO)**2))
WAVCDO=(2.0*PI)*FRO
END
DYNAMIC
* SIMULATION CONTROLS *
ALGORITHM IALGOR=S.JALGOR=S
CINTERVAL CI=.05E-6
NSTEPS NST=2
DERIVATIVE EQS
* PHASE DETECTOR MATH MODEL *
PHIE=PHIR-PHID
PHIR=INTEG(PHIRD.PHIRO)
PROCEDURAL(DELF.IOS.VOS=T.TSTART.FPER.IOFF.VOFF)
DROP
IF(T.GE.TSTART)GO TO L1
DELF=0.0
IOS=0.0
VOS=0.0
GO TO L2
L1..DELF=FPER*FRO
IOS=VOFF
L2..CONTINUE
END
FR=FRO+DELF
PHIRD=2.0*PI*DELF
ID=(SD/RCP)*IOS
SD=VOS*(2.0/PI)*SIN(PHIE)
VPD=((B-1.0)/B)*(1.0/CI)*ID
VP=INTEG(VPD.VPO)
VCP=LEDLAG(TLEAD.TLAG.VP.VCPO)
* BUFFER *
VB=3*VCP
PHIDD=(2.0*PI*KD)*VB
PHID=INTEG(PHIDD.PHIDO)
* VCO MATH MODEL *
CV=CVC+CVT(VB)
TAUVCO=(FDR**2)*(LV*CV)
WAVCO=SQRT(1.0/TAUVCO)
FO=FRO+KO*VB
END
TERMT(T.GT.TFIN)
END
TERMINAL
END TERMINAL
END PROGRAM
```

```
* NONLINEAR MODEL B *
* THIS IS A CHARGE PUMP PHASE LOCK LOOP MODEL *
*TRANSIENT RESPONSE ANALYSIS*
* SYSTEM PARAMETERS *
CONSTANT PI=3.14144.AP= 0.2.RCP=75.0.R1=33.0....
         C1=10.0E-9.CCP=1.0E-9
CONSTANT AMP=1.0.TFIN=15.0E-6.TSTART=0.0
CONSTANT VPO=0.0.VCPO=0.0.PHIRO=0.0.PHIDO=0.0
CONSTANT KD=5.27E+6.KO=2.0
CONSTANT VOFF=0.0.IOFF=0.0.FRO=10.0E+6....
         FPER=0.10.CVO=138.0E-12....
    FVCDO=20.0E+6.CVC=1.0E-12.FDR=2.0
* VARACTOR CAPACITANCE VERSUS VOLTAGE-VB *
TABLE CVT.1.17.-0.7.-0.7.-0.6.-0.5.-0.4.-0.3.-0.2.-0.1....
              0.0.0.1.0.2.0.3.0.4.0.5.0.6.0.7.0.7....
              232.0.232.0.214.0.197.0.182.0.169.0.157.0....
            148.0.138.0.128.0.117.0.109.0.101.0.95.0....
            90.0.87.0.87.0
* NONLINEAR TRANSCONDUCTANCE AMPLIFIER CHARACTERISTICS *
CONSTANT VT=36.0E-3.ICS=2.0E-3
INITIAL
B=1.0+(C1/CCP)
TAU2=(R1+C1)
TLEAD=TAU2
TLAG=(TAU2/B)
CV=CV0
FVCO=FVCDO
LV=(1.0/(CV0+(2.0*PI*FVCO)**2))
WAVCDO=(2.0*PI)*FRO
END
DYNAMIC
* SIMULATION CONTROLS *
ALGORITHM IALGOR=S.JALGOR=S
CINTERVAL CI=.05E-6
NSTEPS NST=2
DERIVATIVE EQS
* PHASE DETECTOR MATH MODEL *
PHIE=PHIR-PHID
PHIR=INTEG(PHIRD.PHIRO)
PROCEDURAL(DELF.IOS.VOS=T.TSTART.FPER.IOFF.VOFF)
DROP
IF(T.GE.TSTART)GO TO L1
DELF=0.0
IOS=0.0
VOS=0.0
GO TO L2
L1..DELF=FPER*FRO
IOS=IOFF
VOS=VOFF
L2..CONTINUE
END
FR=FRO+DELF
PHIRD=2.0*PI*DELF
SD=VOS*(2.0/PI)*ASIN(PHIE)
VPD=((B-1.0)/B)*(1.0/CI)*ID
ID=IOS*ICS*((EXP(AID)-1.0)/(EXP(AID)+1.0))
AID=2.0*(SD/VT)
VP=INTEG(VPD.VPO)
VCP=LEDLAG(TLEAD.TLAG.VP.VCPO)
* BUFFER *
VB=3*VCP
PHID=INTEG(PHIDD.PHIDO)
PHIDD=WAVCDO*KVCDO
* VCO MATH MODEL *
CV=CVC+CVT(VB)
TAUVCO=(FDR**2)*(LV*CV)
WAVCO=SQRT(1.0/TAUVCO)
FO=WAVCO/(2.0*PI)
END
TERMT(T.GT.TFIN)
END
TERMINAL
END TERMINAL
END PROGRAM
```

Fig.10 : CSSL-IV Program for a) Linear Model
b) Nonlinear Model



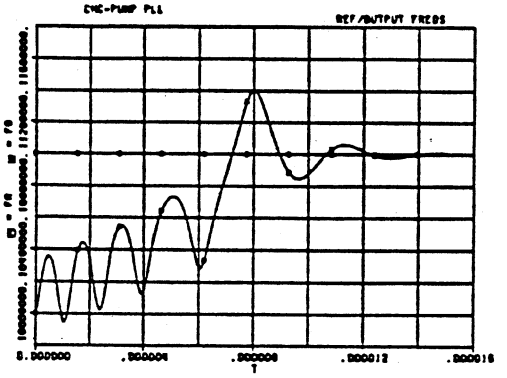


Fig.11 : Step Input Response of the Analog CP-PL for a) Linear Model b) Nonlinear Model with Linear Charge Pump (R_{cp}=150 ohms)

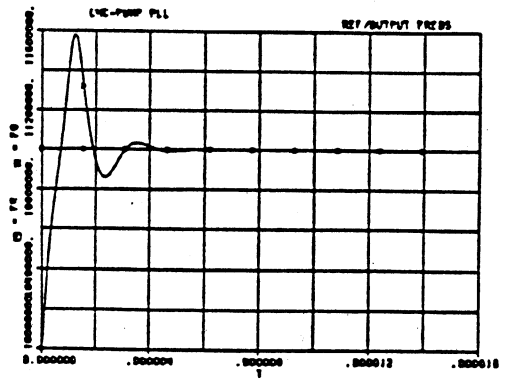


Fig.12 : Step Input Response of Analog CP-PLL for Nonlinear Model with Linear Charge Pump (R_{cp}=75 ohms).

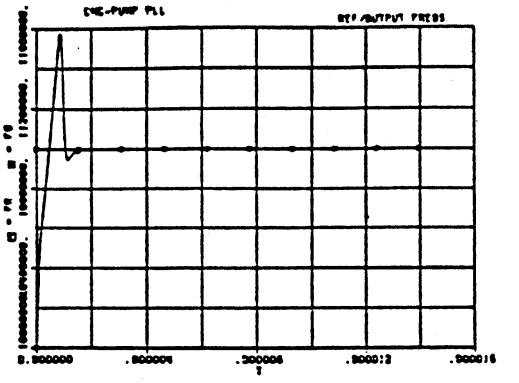
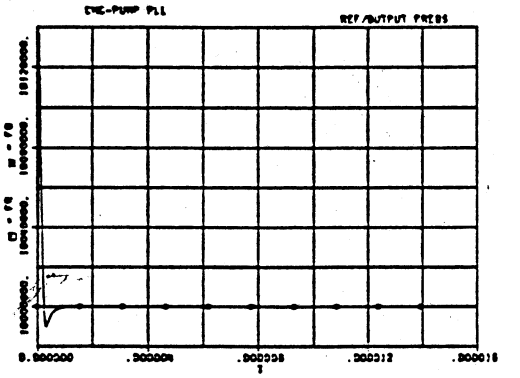


Fig.13 : Step Input Response of Analog CP-PLL for Nonlinear Model with Nonlinear Charge Pump [R_{cp}=0 , I_{cp}=I_{cs} Tanh(.)].



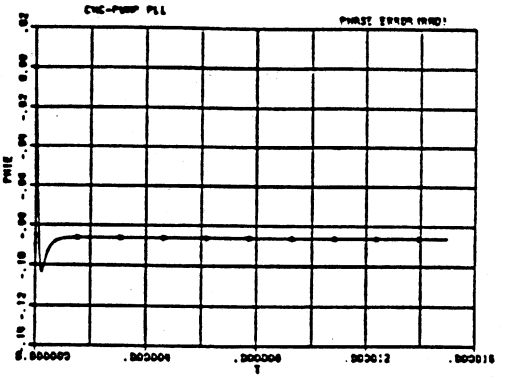


Fig.14 : a) Step Input Response of Analog CP-PLL for Nonlinear Model with Offsets b) Phase Error with Offsets (V_{os}=10mV , I_{os}=75μA).