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CUSTOM LINEAR INTEGRATED CIRCUIT DESIGN TECHNIQUES

Ted Bee, Sumer Can
Integrated Circuit Design, Santa Clara, CA

1. INTRODUCTION

A custom VLSI circuit is described which contains a number of circuits which are representative of typical building block functions encountered in linear systems. It will be shown how a system containing a considerable number of discrete standard off-the-shelf ICs can be realized in a single chip by using certain design techinques to simplify the circuit, in some cases to economize on silicon area, and to overcome problems and limitations in processing the signal by conventional means. Emphasis will be placed on the circuit description rather than on system understanding for more general applicability to circuit designs for other systems.

Criteria for justification of custom IC design are packaging (space saving), cost effectiveness, performance and reliability, and these features are discussed in the following section.

2. SYSTEM OUTLINE

Figure 1 shows the elements in the discrete system design in which a differential signal is received from a servo magnetic head pre-amplifier and gain-multiplied through a wide band amplifier, filter and AGC block. Sequential pulses are gated and peak detected on four peak hold capacitors which will track the changing amplitude of each channel, A to D. The voltages on the peak hold outputs are summed and averaged to control the gain of the AGC amplifier to give a constant output for the maximum peak voltage. The differences of the amplitudes between channels A & B and C & D can be selected by the multiplexer and used to give a position error.

It can be seen that this system uses the equivalent of fourteen discrete ICs plus a complex discrete transistor circuit for gating and peak detection. In addition, other features in the custom chip (Figure 2) include a digitizer for obtaining a digitized servo carrier output. Thus packaging and cost saving objectives are realized, especially if assembly and part ordering costs are considered. Reliability follows from reduced parts count and less soldered joints, provided the IC is designed carefully! In an integrated approach, certain performance advantages can be obtained in terms of minimizing setting up adjustments, signal processing speed and having tailor-made parameters designed to match the system requirements.

The initial challenges from a design point of view were contained in the realization of the very fast peak detectors and wide band high slew rate of the servo carrier signal, which in the discrete design uses an amplifier with a dielectric isolation process. A different method was used in the custom design to achieve the signal multiplexing, which is done by switching voltages in the discrete design. The custom design converts the voltages to currents which are then switched and subtracted to give the difference signals.

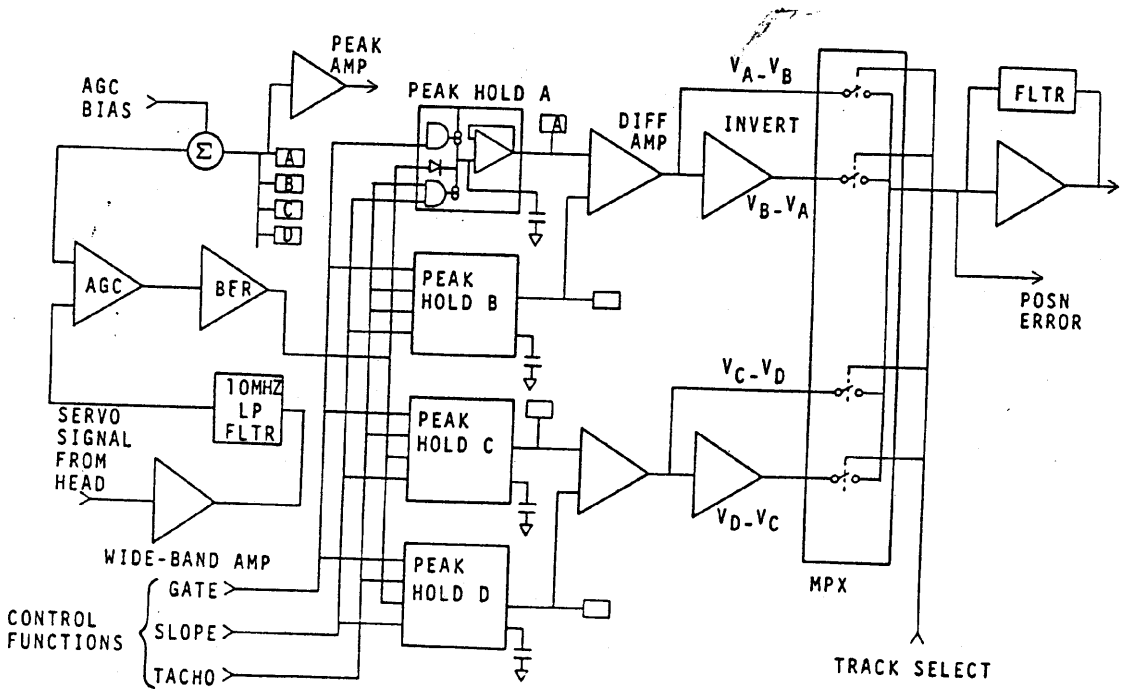


FIGURE 1. SERVO SYSTEM FUNCTIONAL SCHEMATIC

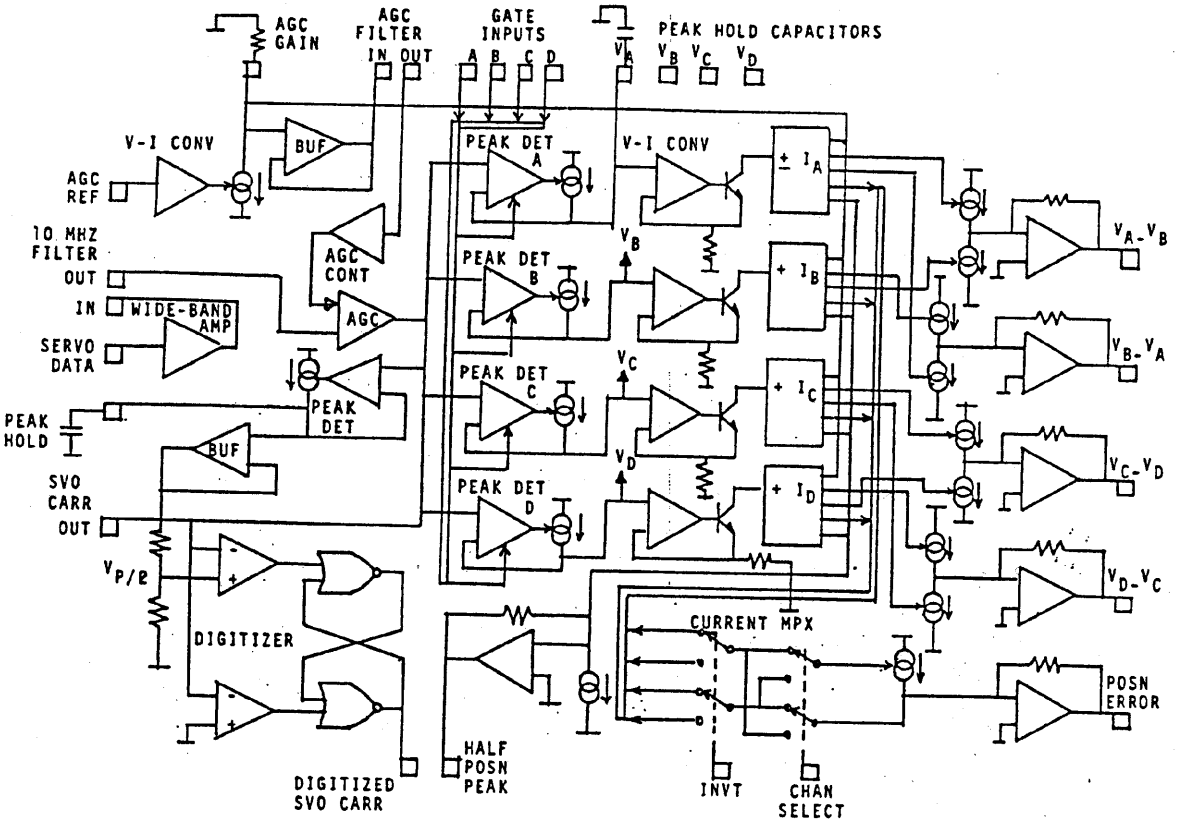


FIGURE 2. SIMPLIFIED FUNCTIONAL SCHEMATIC OF CUSTOM I.C.

3. CIRCUIT DESIGN

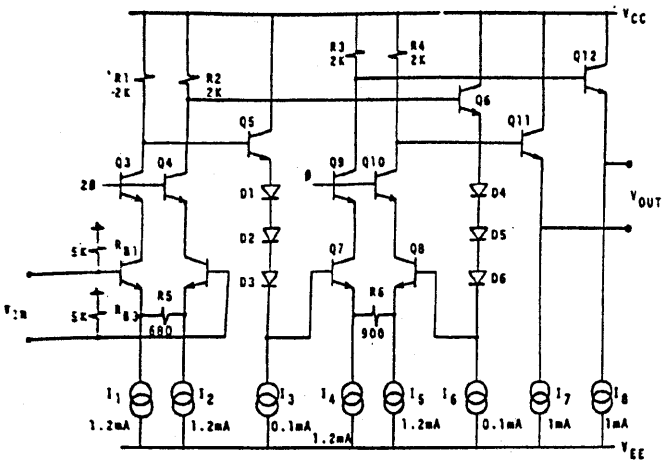
3.1. General

The features of integrated circuit design make use of the inherent close matching of transistors and resistor ratios, consequently an IC circuitry looks completely different from discrete circuit design. Limitations occur in the maximum current handling properties of transistors, NPNs of minimum geometry being limited to the order of 1 ma and PNPs of minimum geometry having a maximum current of 100 ua before current gain (β) degradation sets in. In addition, PNPs have a much reduced operating frequency limit (f_t) compared to NPNs. Consideration must be paid to the wide tolerance of resistors (generally $\pm$20%) and the optimum values from the point of view of layout. As a general guideline, values of less than 100 ohms and greater than 10K tend to use an undesirable amount of silicon, although this requires some judgment and tradeoff. Also, it is possible to integrate NPNs which can handle more than one ampere, at the cost of silicon area and power dissipation. The IC is designed to operate at nominal supply voltages of +5V V_{cc} and -5V VEE. The appendix contains a review of some useful equations and terms used in linear IC design.

3.2. Wide-Band Amplifier

The wide-band amplifier (Figure 3) is a two stage differential amplifier designed to deliver a maximum 2V peak differential output signal at 10 MHZ with minimum distortion. The values of R3, R4 are limited to 2K to reduce the effect of parasitic capacitances on the frequency response at Q9, Q10 collectors. The operating d.c. voltage level of 2.5V is set by constant current sources I_4, I_5 of value 1.25ma to enable a 1V peak voltage swing on the outputs. The gain of the stage is set by approximately $(R_3 + R_4)/R6$. To keep distortion at a minimum, it is necessary that the input signal to the stage across the bases of the differential pair Q7, Q8 appears across the emitter degeneration resistor R6 with minimum modulation of the emitter-base voltages of Q7, Q8. It can be seen that the quiescent current through Q7, Q8 changes only $\pm$0.5ma in 1.25ma at full signal swing. A simple way of predicting gain change with signal level of a differential amplifier is shown with reference to Figure 4, where r_{e1} and r_{e2} represent the small signal dynamic emitter resistances of Q1 and Q2, which at balance are equal. Now $r_{e1} = V_T/I_1$, where V_T = 26mv at room temperature. Thus at balance, the total emitter resistance which is $r_{e1} + R_E + r_{e2}$ will be 941 ohms for the second stage in question. This will change to 950 ohms at maximum signal when the current through Q1 is 1.25ma and the current through Q2 is 0.75ma. Thus the gain change of the amplifier is only 0.9% with maximum signal. The function of Q9 and Q10 cascode transistors in Figure 3 is to isolate the effect of the collector-base junction capacitance of the input differential pair Q7, Q8 from the output. Otherwise, the junction capacitance will be multiplied by the voltage gain of the stage. Cascode transistors Q9, Q10 do not affect the gain of the stage because the output collector current is effectively equal to the input emitter current.

D.C. level shift between the first and second stages is accomplished through Q5, D1, D2, D3 and Q6, D4, D5, D6 which are supplied by constant current sources I3 and I6. High input impedence transistors Q5 and Q6 provide minimum loading for the output of the first stage, which is similar design to the second stage. The overall voltage gain of the amplifier is 20. RB1, RB2 provide the base current path for Q1, Q2 and effectively set the input impedence of the amplifier as the impedence across Q1, Q2 is R5 multiplied by the current gain

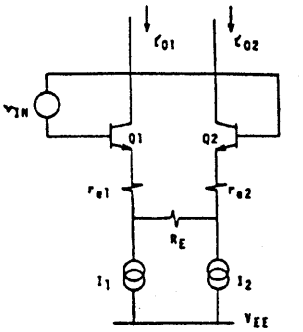


WIDEBAND AMPLIFIER
FIGURE 3.

(I_C/I_B)of the transistor. Output transistors Q11, Q12 provide low output impedence equal to R3 divided by the transistor current gain.

3.3. A.G.C. Amplifier

The input signal of maximum value 0.2V peak to the A.G.C. amplifier shown in Figure 5 is buffered by high impedence unity gain amplifiers Q1, Q2, Q3 and Q4, Q5, Q6 such that the input signal appears across R1 and R2 with minimum loss. The differential current across R1, R2 will be transferred through Q3, Q6 to diodes D1, D2. The diode D3 will have constant current I3 through it and will therefore have no A.C. signal across it. From the basic diode equation, the voltage differential across D1, D2 which is applied across differential pair Q7 and Q8, will result in the current through Q9 being modulated by the same amount as I3. The resulting signal will appear across R3, R4. The resulting gain will thus be R3.I6/R1.I3. The advantage of this type of stage, known as a Gilbert Cell [1], is that the signal levels across the diodes are kept small, to minimize distortion. Another way of looking at this is to say that the load impedence of the first stage (diodes D1, D2) is an inverse function of I3 and the g_m of the second stage is a function of the current through Q9 (I_{Q9}). The g_m of the first stage being R1 + R2, its voltage gain is $\frac{V_T}{I3} \cdot \frac{1}{(R1 + R2)}$. The voltage gain of the second stage is (R3 + R4) I_{Q9}/V_T resulting in the overall gain given above.



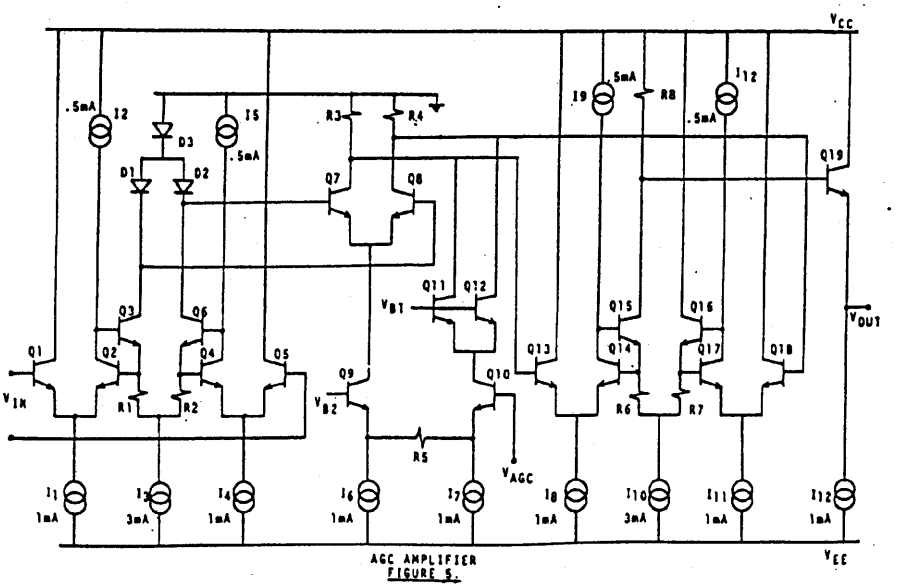
GAIN OF SIMPLE DIFFERENTIAL AMPLIFIER WITH EMITTER DEGENERATION RESISTANCE
FIGURE 4

Thus the gain is controlled by changing the current through Q9, by means of applying a differential voltage across Q9, Q10. The d.c. level on R3, R4 is maintained constant by means of Q11, Q12 splitting Q10 current evenly into R3, R4.

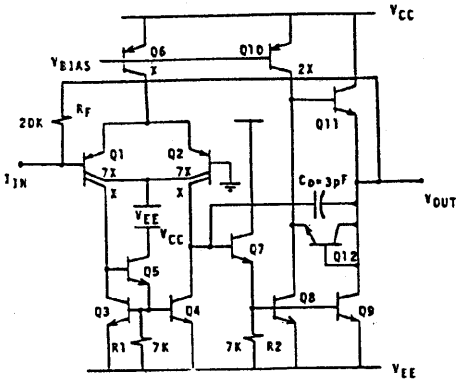
Another stage of amplification is necessary, by a similar circuit to the input stage, to give a gain of X10 to a single ended output.

3.4. Peak Detector

The output voltage of the AGC amplifier is applied to the input of the peak detector shown in Figure 6. The peak amplitude of the input voltage is stored on the external capacitor C. The gate input on Q8 serves to make the differential pair Q1, Q2 active only during the desired period by switching the selected charging current I1 or I2 to the differential amplifier through Q6. In the active mode, one third of the charging current will be diverted to the PNP current mirror Q3, Q4, Q5 through Q7. Q3 acts as a current source of value equal to the current supplied to Q4 collector. If V_{IN} is greater than V_{OUT}, then Q2 current will be less than Q3 current and the net difference will go into the current mirror Q9, Q10, Q11 and be multiplied by times 20 by Q10. The output current from Q9, Q10 emitters will charge the capacitor C through Schottky diode D1 until V_O becomes equal to V_{IN}. At this point, the differential amplifier will be balanced and Q1 and Q2 currents will be equal, and Q3 current will be equal to Q2 current. The charging current through Q10 will be zero. Note that the capacitor can only charge quickly in a positive direction because of D1. I3 is a small discharge current designed to reduce the voltage on C between gating periods in a certain mode of operation, when SLOPE input is low with respect to V_{REF}.



AGC AMPLIFIER
FIGURE 5.



CURRENT TO VOLTAGE CONVERTER (OP. AMP.)
FIGURE 9

currents as described in the previous section. Some interesting features of this circuit are contained in the output stage which is all NPN, giving good frequency response. The biasing is arranged so that at zero volts on the output, Q11 and Q9 are both in conduction so that a smooth transition is obtained going from positive to negative output voltages. The value of the quiescent Q11, Q9 current at cross-over is obtained from constant current source Q10, which with no signal will force Q8 to be of equal value and consequently Q9 to be of the same value.

For negative going output swings, Q7 will drive Q8, Q9 on, and Q12 will conduct, turning off Q11. For positive output voltages, Q7 will turn off, reducing the current from Q8, Q9 collector. The net difference between Q10 constant current (=200 ua) and Q8 will go into Q11 and be gain multiplied into the output load.

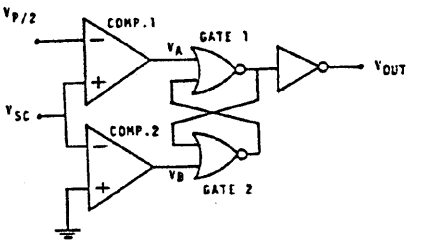
The op-amp can be considered to be a two stage design, the input stage up to Q7 base having a gain of g_m ($= {}^{I_O}/_{V_{IN}}$) of value determined by Q6 constant current source and the ratio of the collector areas. The output stage can be considered as a high gain voltage amplifier. Across the stage there is an internal compensation capacitor, which is a MOS type of value 3pf. The output current of the first stage will be forced through this capacitance when its impedence is less than the input impedence of Q7. Thus the open loop gain of the amplifier will be g_m/sC which will produce a well defined 6dB/octave roll-off, ensuring unconditional stability under all feedback conditions. This is provided that there are no other breakpoints in the open loop frequency response before gm/sC becomes equal to 1, the frequency point of which determines the bandwidth of the amplifier.

Q3, Q6, Q5 serves as an active load for the output of the differential pair Q1, Q2 so that the change in output current from Q1 is reflected in Q4, doubling the net output current change into Q7.

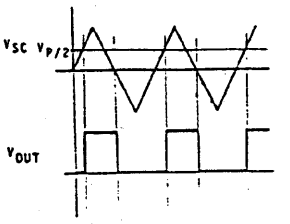
The available output voltage swing will be the supply voltages less 2 ($V_{BE} + V_{SAT}$).

3.8 Digitizer

A digitizer circuit is also included in the custom IC for obtaining a digitized servo carrier output. Block structure of the digitizer is shown in Figure 10.a which contains two fast comparators, two cross coupled nor gates and a TTL compatible output stage. Functional description of the digitizer is also presented as a table in the same figure. Simplified circuit schematic is given in Figure 10.b. In this figure, Q1, Q2 and Q3, Q4 are the differential pairs for comparator 1 and comparator 2, in which the non-inverting input terminal of comparator 1 is connected to the inverting input terminal of comparator 2 where the servo carrier signal is applied. The threshold voltages for the comparators are set as $V_P/2$ and zero by applying $V_P/2$ signal to the inverting input



V_{SC}	V_A	V_B	V_{OUT}
<0	L	H	L
0	L	L	L
$V_{P/2}$	H	L	H
V_P	H	L	H
$V_{P/2}$	L	L	H
0	L	H	L
<0	L	H	L



DIGITIZER BLOCK STRUCTURE
FIGURE 10.A.

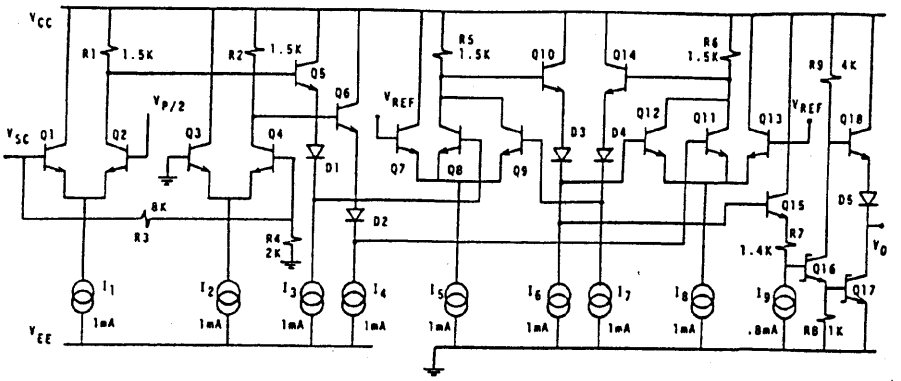
terminal of comparator 1 and connecting the non-inverting input terminal of comparator 2 to ground. The outputs from the comparators are level shifted by Q5, D1 and Q6, D2. Gate 1 and Gate 2 are realized by Q7, Q8, Q9 and Q11, Q12, Q13. The base of Q7 and Q13 are kept at a reference voltage level and the switching is achieved by bringing the base of Q8 (Q11) or Q9 (Q12) Ø volt above or below around this reference level. The base of Q8 and Q11 are the inputs driven by comparators while two gates are cross-coupled through the base of Q9 and Q12, after a level shifting by Q10, D3 and Q14, D4. The output stage is driven from the base of Q15. After further level shifting through R7, the Schottky clamped transistor Q16 is driven. When Q16 is on, a current flows through R9, Q16 and R8 causing Q17 to turn on. At the same time, voltage drop across R9 keeps Q18 off. When Q16 is turned off, Q17 turns off and the base of Q18 goes to supply causing Q18 to turn on. Thus, a TTL compatible output, which is called digitized servo carrier output, is obtained.

3.9. Reference For Current Source Biasing

An interesting method of biasing the constant current sources is shown in Figure 11. Consider that R5 and R6 have equal voltages across them (each end sees $2V_{BE}$ to V_{EE}) and consequently, Q6 will have ten times the current that Q8 has. But a current ratio of 10:1 means for equal area transistors, a difference of V_{BE} of 60 mV (at room temperature). This V_{BE} will appear across R4 and define the current through Q8 and consequently through R6. The voltage on Q7 emitter will therefore be the V_{BE} of Q9 and Q10, plus $\frac{V_{BE}\,(Q6 - Q8)\,R6}{R_4}$.

The result is that across R5, there is a voltage 60mV . R6/R4, defining the current into Q6 and consequently the currents in all NPN transistors connected to bias line A. These currents will track with temperature because V_{BE} increases with temperature, as do integrated resistor values.

Q9, Q12 serve to bias the base of Q7 at the correct voltage.



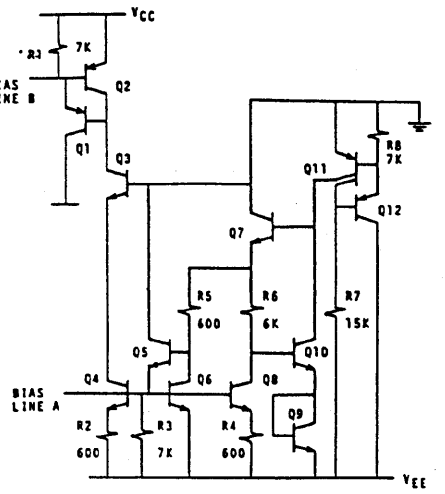
DIGITIZER
FIGURE 10B

PNP current source references with respect to V_{CC} are obtained from Q6 supplying a constant 0.1ma to Q2 through Q3 cascode transistor, which reduces the voltage on Q6 collector. Then all PNP current sources connected to bias line "B" can be referenced to Q2. The base currents of the PNP current sources are supplied by Q1.

Similarly, the base currents of all NPN current sources connected to "A" are suppled by Q5.

4. C.A.D.

In a circuit of this complexity, it was necessary to make extensive use of CAD analysis to verify the circuit operation. SPICE was used for this purpose and enabled D.C. conditions, A.C. linear frequency response and transient performance to be examined. Apart from the inevitable "bugs" inherent in breadboards, at high frequencies parasitic capacitances become a limitation. With computer simulation, worst case tolerancing can be performed. Also, aspects of circuit parameters, such as currents and high impedence point voltages, can be more easily examined. However, it is necessary to have an analytical understanding of the circuit as the computer will only point out the results of any changes made in the parameters.



REFERENCE FOR CURRENT SOURCE BIASING
FIGURE 11

5. PROCESS

The IC has been designed for the STTL20 linear process developed by the Univac Semiconductor Division at Eagan. This process is very fast (1 - 2 GHZ), with dual layer metal and self-aligning diffusion layer to minimize diffusion clearances. Base sheet resistance is 200 ohms. Maximum voltage is 12V.

6. LAYOUT

The IC is designed for a 44 pin D.I.L. package and contains 547 transistors.

Figure 12 shows the relative dimensions of different structures, The PNP (12 a) has split collectors of ratios 3:1 of rather unique design to maximize collection of emitter current. This device is good for about 100 ua and is larger in area than the 1 ma NPN shown in (12 c). The relative emitter areas of the NPNs shown in 12(b) and 12(c) are 1:10.

It can be seen that the 20K ohm resistor takes up by far the greatest amount of silicon.

A section of the layout which comprises the peak detector circuit is shown in Figure 13.

7. SUMMARY

By combining a limited number of elemental building blocks, a variety of different circuit functions can be realized in economical form. In many cases, an op. amp. for example, the circuitry can be greatly simplified to suit the application, rather than having to meet a wide variety of general requirements as would a standard general purpose IC.

8. APPENDIX

A brief recap of the elements of linear design may be in order to highlight some aspects of the circuits described in this paper. The relationships given will be correct to a first order of magnitude.

Basic to linear IC design is the extensive use made of the fundamental diode equation:

$$\ln(I_E/I_S) = qV_{BE}/kT \qquad (8.1)$$

where

I_E = emitter current
I_S = saturation current (very low value)
q = electronic charge (1.6×10^{-19} C)
h = Boltzmann constant (1.38×10^{-23} $J^{\circ}K^{-1}$)
T = temperature in degrees Kelvin

V_{BE} = base emitter voltage

At room temperature, (300°K)

Thermal voltage V_T = 26 mV

This equation is useful because of the matching of the transistors which will therefore have equal values of saturation current, I_S (for equal emitter area devices). This term has a temperature dependence, but it is generally assumed that devices placed close together on the chip will be at the same temperature, hence the close attention paid in laying out matched transistors next to each other where possible.

Taking equation (1) for equal area devices and dividing the expressions for emitter current, we find:

$$V_T \cdot \text{Ln} \left({}^{I_{E1}}/_{I_{E2}} \right) = V_{BE1} - V_{BE2} \qquad (8.2)$$

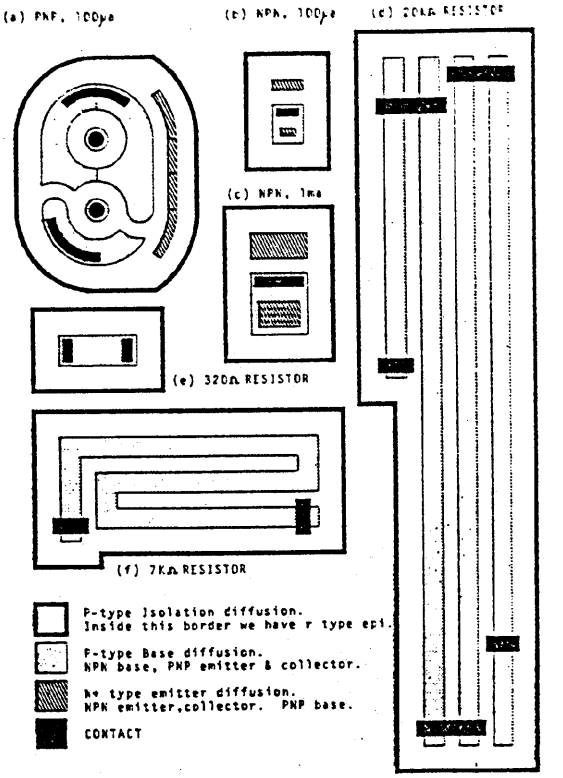
This very interesting expression reveals the fact that a given difference in base emitter voltage will correspond to a certain emitter current ratio, independent of the actual currents, provided of course that they are within the linear operating range of the transistor. Thus it can be assumed that, for example, 60mV V_{BE} corresponds to a 10:1 current ratio, and 18mV corresponds to a 2:1 ratio, and so on.

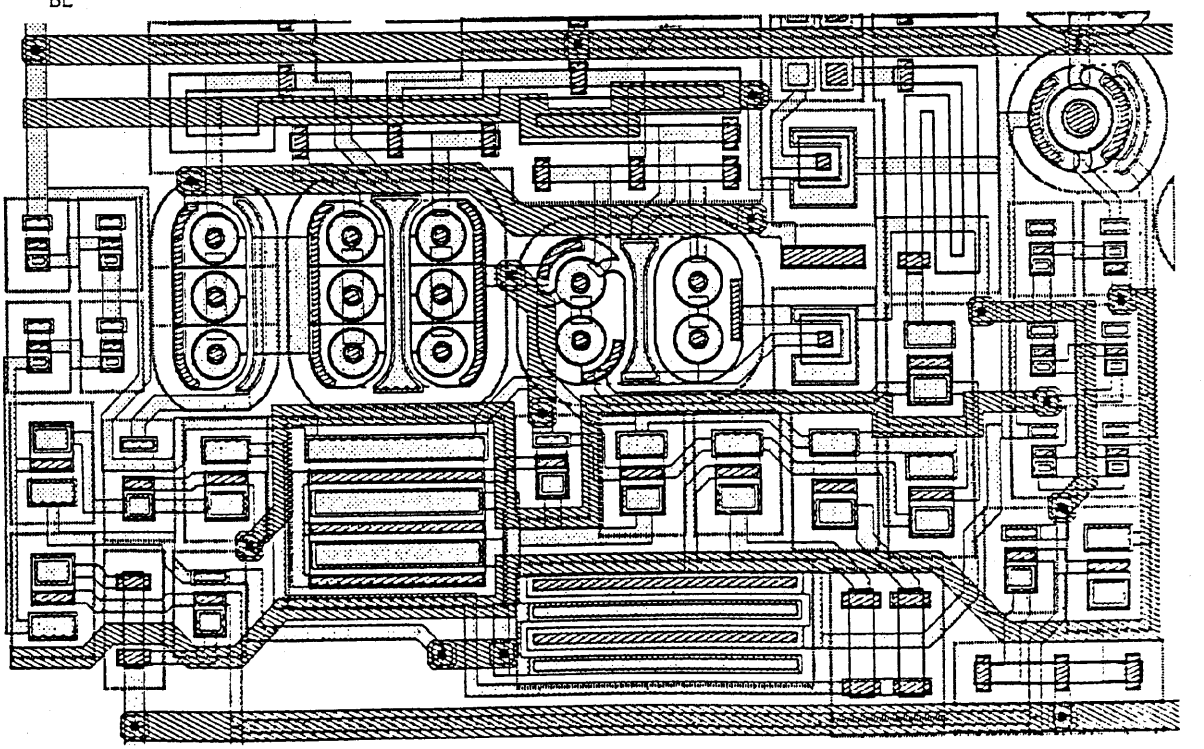
Furthermore, because I_S is proportional to transistor emitter area, it follows that a transistor with ten times the emitter area of another one will have a V_{BE} 60 mV less for the same emitter current, and so on. (I_S is ten times larger.)

Referring back to equation (1), and differentiating I_E with respect to V_{BE}, we obtain an expression for the mutual conduction (gm) of a transistor:

$$\frac{d(I_E)}{d(V_{BE})} = {}^{V_T}/_{I_E} \text{ where } I_E \text{ is the emitter current} \qquad (8.3)$$

FIGURE 12. RELATIVE DIMENSIONS OF DEVICES





A SECTION OF THE LAYOUT: PEAK DETECTOR
FIGURE 13

Thus, a transistor biased at 1 ma will have a g_m of 1/26 mhos, or an r_e of 26 ohms. (r_e can be regarded as a fictitious resistor in the emitter of a transistor, and is useful in estimating the voltage gain of a transistor, together with other properties.)

Figure 14 shows some useful relationships for different configurations of transistor bias.

Extensive use is made of transistor matching in current sources, as shown in Figure 15. Here it can be assumed that identical transistors with equal base-emitter voltages will have equal collector currents. (There will tend to be a second order error due to finite output impedence of the devices.)

Inclusion of emitter resistors has the effect of increasing output impedence of the current source.

In the case of PNP transistors, it is possible to ratio the collector areas, because of the way they are constructed, to obtain the desired current source ratios from one device. Thus PNPs can be multi-collector devices, whereas NPNs can be multi-emitter.

In practice, the f_t where the current gain ($\beta = \frac{I_C}{I_B}$) falls to unity, is a function of the current bias level of the device. At low currents, f_t tends to decrease quite rapidly. Above a certain maximum current density, the current gain β will decrease from a maximum value and it is desirable not to operate a transistor in this region.

Consideration must also be paid to temperature effects, which most notably affects V_{BE}, β and r_e.

FIGURE 14 PROPERTIES OF TRANSISTOR BIAS CONFIGURATIONS

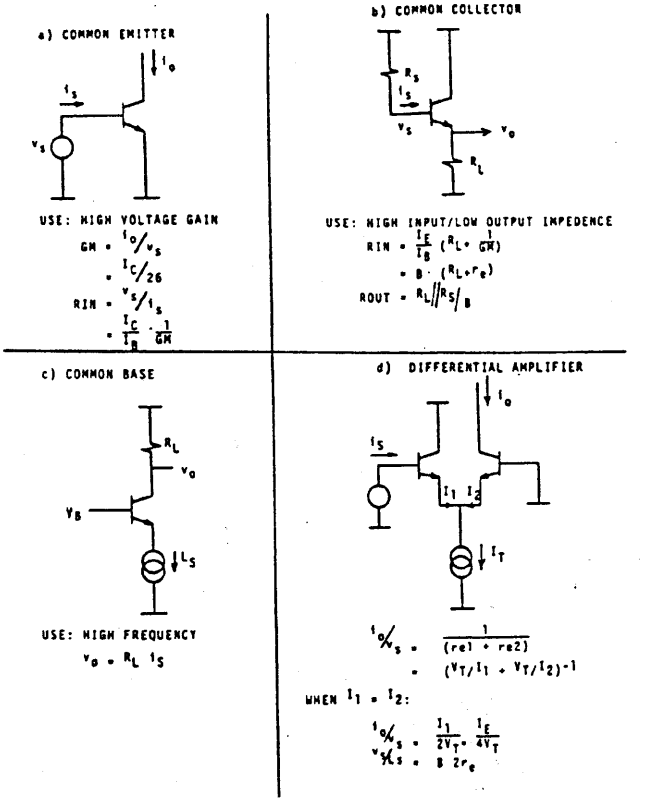


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FIGURE 15. CURRENT SOURCE BIASING, USE OF CURRENT MIRRORS